Application Note

BRT_AN_019

FT90x Revision B to Revision C - Migration Guide

Version 1.1

Issue Date: 2017-11-01

This application note lists out the changes between FT90x Revision B and FT90x Revision C. It also contains the details that the user needs to be aware of for a smooth migration to FT90x Revision C.

Bridgetek Pte Ltd (BRTChip)
178 Paya Lebar Road, #07-03 Singapore 409030
Tel: +65 6547 4827 Fax : +65 6841 6071
Web Site: http://brtchip.com

Table of Contents

1 Introduction 3
2 Change Summary 4
3 Electrical Specification Change in FT90x Revision C .. 6
3.1 FSOURCE Pin 6
3.2 VPP Pin 6
3.3 VBAT Pin 6
4 Functional Change in FT90x Revision C 7
4.1 RTC 7
4.2 ADC 7
4.3 DAC 7
4.4 Timers 8
4.5 PWM 8
4.6 CAN Bus Controller 8
4.7 Ethernet 9
4.8 SPI 9
4.9 UART 10
4.10 USB Peripheral 10
4.11 USB Host 10
4.12 Watchdog 11
5 PCB Design suggestions to retain compatibility with both revisions 12
5.1 FSOURCE and VPP 12
5.2 VBAT 12
6 Contact Information 13
Appendix A – References 14
Document References 14
Acronyms and Abbreviations 14

Appendix B – List of Tables & Figures 15

List of Tables.....15

List of Figures 15

Appendix C – Revision History 16

1 Introduction

The FT90x Revision C introduces several changes over the previous version, which aims to improve the performance and add functionality. While efforts have been made to ensure the FT90x Revision C is compatible with existing hardware and software, the changes do require some attention. This document contains details about these changes. It also contains the details that the user needs to be aware of for a smooth migration from FT90x to FT90x Revision C.

2 Change Summary

Change	Short Description	Remarks
Pin 32 (100-pin QFN/LQFP) Pin 20 (76-pin QFN) Pin 23 (80-pin LQFP)*	FSOURCE on FT90x Revision B. In revision C, this must be tied to +1.2V regulator power output (100 and 80-pin packages) or NC (76-pin package). Also connect a 0.1uF decoupling capacitor to GND for 100 and 80-pin packages.	This may require hardware change if the pin has been connected to a different voltage level.
Pin 33 (100-pin QFN/LQFP) Pin 21 (76-pin QFN) Pin 24 (80-pin LQFP)*	VPP on FT90x Revision B. In revision C this must be tied to 3.3V supply voltage (100 and 80-pin packages) or +1.2V regulator power output (76-pin package). Also connect a 0.1uF decoupling capacitor to GND.	This may require hardware change if the pin has been connected to a different voltage level.
Pin 86 (100-pin QFN/LQFP) Pin 67 (76-pin QFN) Pin 71 (80-pin LQFP)*	NC on FT90x Revision B. In revision C, this pin is used to provide external battery power for the RTC.	This may require hardware change if the RTC is used in Revision C.
New RTC IP	The RTC in FT90x Revision B is a simple counter. It provides information as a basic "system on" timer. The RTC in FT90x Revision C has been redesigned to provide more detailed information. It is powered by an external battery source.	This may require hardware change to provide the necessary power for the RTC. The software needs to support the new RTC. API libraries are provided with the latest toolchain.
ADC	IP improvements. The internal Op-amp has been removed.	For Revision C, the user may choose to include an external Op-amp for the ADC to improve the performance.
DAC	IP improvements	No hardware change is necessary. The software needs to be updated to support the extra features if desired. For more information about the features, please refer to the details in the corresponding section.
Timers	IP improvements	
PWM	IP improvements	
CAN	IP improvements	
Ethernet	IP improvements	
SPI	IP improvements	
UART	IP improvements	

Change	Short Description	Remarks
USB Device	IP improvements	
USB Host	IP improvements	
Watchdog	IP improvements	

Table 2.1 - Change Summary

(*) Refer to the tables below for the actual part numbers.

Part Number	Package
FT900Q/FT901Q/FT902Q/FT903Q	100-pin QFN
FT900L/FT901L/FT902L/FT903L	100-pin LQFP
FT905Q/FT906Q/FT907Q/FT908Q	76-pin QFN
FT905L/FT906L/FT907L/FT908L	80-pin LQFP

Table 2.2 - FT90x Revision B Part Numbers

Part Number	Package
FT900Q-C/FT901Q-C/FT902Q-C/FT903Q-C	100-pin QFN
FT900L-C/FT901L-C/FT902L-C/FT903L-C	100-pin LQFP
FT905Q-C/FT906Q-C/FT907Q-C/FT908Q-C	76-pin QFN
FT905L-C/FT906L-C/FT907L-C/FT908L-C	80-pin LQFP

Table 2.3 - FT90x Revision C Part Numbers

3 Electrical Specification Change in FT90x Revision C

3.1 FSOURCE Pin

Introduction:

The FT90x Revision B has an FSOURCE input pin to provide power for programming the 64-bit EFUSE. Typically, FSOURCE has to be at +3.70V while the EFUSE is being burnt.

Change in FT90x Revision C:

The EFUSE has been removed; hence there is no longer a need for the FSOURCE pin.

In Revision C, 100 and 80-pin packages, this pin is a 1.2V input pin to provide extra noise immunity to the internal PLL. A 0.1uF decoupling capacitor to GND should be connected. For the 76-pin package, this pin should be NC.

For 100 and 80-pin packages, this pin is connected to the 1.2V regulator output on the chip die. It is suggested that a 1.2V power plane is provided on the PCB to minimize the power drop and noise at 1.2V pins.

3.2 VPP Pin

Introduction:

The FT90x Revision B has a VPP input pin to provide power for programming the 64-bit EFUSE. Typically, VPP has to be at +1.85V while the EFUSE is being burnt.

Change in FT90x Revision C:

In FT90x Revision C, the EFUSE has been removed; hence there is no longer a need for the VPP pin. For 100 and 80-pin packages, the pin should now be connected to 3.3V to provide power for the chip. For 76-pin packages, it should be connected to the 1.2V regulator output on the chip die. It is suggested that a 1.2V power plane is provided on the PCB to minimize the power drop and noise at 1.2V pins. A 0.1uF decoupling capacitor to GND should also be connected to this pin for all packages.

3.3 VBAT Pin

Introduction:

The FT90x Revision B does not have a power pin to connect a battery to the RTC. The RTC on Revision B will not function when the power to the system is cut off.

Change in FT90x Revision C:

In FT90x Revision C, a battery can be connected to the RTC via the VBAT pin so that it can continue working even when the system is powered off.

4 Functional Change in FT90x Revision C

4.1 RTC

Introduction:

The Real Time Clock (RTC) provides separate Second, Minute, Hour, Day, Date, Month and Year with Leap Year information in BCD format. The clock may also be configured into 24-hour or 12-hour format with an AM/PM indicator. There is additional provision for an On-Chip Digital Trimming/Calibration facility that can be used to adjust for the frequency variance caused by crystal tolerance and temperature. It is clocked by a 32.768 kHz external oscillator.

For more information on the new RTC, please refer to BRT_AN_020_FT90x_Revison_C_User_Manual.

Change in FT90x Revision C:

The RTC in FT90x Revision C has been totally redesigned. It provides more meaningful information about date and time. It is powered by an external 1.5V battery instead of the internal 1.2V regulator as in the FT90x Revision B. Existing boards may need to be updated to facilitate the external battery source if the RTC is used.

4.2 ADC

Introduction:

The ADC in FT90x Revision C is similar to the ADC in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

- The FIFO Data Count issue, as stated in TN_159 FT90x Errata Technical Note, section 4.3, has been fixed. Counts of 0x7E and 0x7F now appear correctly, and 0xFF indicates the FIFO is empty.
- A bit has been added to select the size of the ADC samples: either 10 bits or 8 bits.
- A bit has been added to select the ADC clock speed: 12.5 MHz or 6.25 MHz.
- The internal Op-amp has been removed.

4.3 DAC

Introduction:

The DAC in FT90x Revision C is similar to the DAC in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The FIFO Data Count issue, as stated in TN_159 FT90x Errata Technical Note, section 4.4, has been fixed. Counts of 0x7E and 0x7F now appear correctly, and 0xFF indicates the FIFO is empty.

4.4 Timers

Introduction:

The Timers in FT90x Revision C are similar to the Timers in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The issue described in TN_159 FT90x Errata Technical Note, section 4.1, has been fixed as follows:

To read or write the registers, always start with the lower 8-bits followed by the upper 8-bits. For write, the actual write occurs only after the upper 8 bits are written. To read, the upper 8-bits are held in a temporary location when the lower 8 bits are read. Writing/reading the upper 8-bits without accessing the lower 8-bits first may produce erroneous write/read to/from the registers.

4.5 PWM

Introduction:

The PWM in FT90x Revision C is similar to the PWM in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

Issue 2 as described in TN_159 FT90x Errata Technical Note, section 4.2, has been fixed as follows:

For write operations, the LSB must be written first. Only when the MSB is written will the full 16-bit data get transferred to the MSB and LSB registers together. If the MSB is written without the LSB being written first, the LSB assumes the value 0.

For read operations, the LSB must be read first. The MSB will be held in a temporary register that can be read with a subsequent MSB read. It is not recommended to read the MSB of a 16-bit register without first performing the corresponding LSB read. The MSB value should be treated as undefined in such cases.

4.6 CAN Bus Controller

Introduction:

The CAN Bus Controller in FT90x Revision C is similar to the CAN Bus Controller in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The issues described in TN_159 FT90x Errata Technical Note, section 4.6, have been fixed. The details are as follow:

- Issue 4.6.1: When the exception occurs, the TRANSMIT ERROR COUNT is increased (by 8) once.
- Issue 4.6.2: The 'error passive' station now waits for six consecutive bits of equal polarity, beginning at the start of the PASSIVE ERROR FLAG.

- Issue 4.6.3: When the OVERLOAD condition 1 occurs, the CAN controller sends the OVERLOAD FRAME immediately after the End of Frame.

Regarding issue 4.6.3 in the Errata, 3 additional bits are also added in the CAN registers:

- CAN_STATUS[4]: this bit indicates the data overload status
- CAN_INT_STATUS[7]: this bit indicates the data overload interrupt status
- CAN_INT_ENABLE[7]: this bit enables/disables the data overload interrupt

4.7 Ethernet

Introduction:

The Ethernet in FT90x Revision C is similar to the Ethernet in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The limitation described in TN_159 FT90x Errata Technical Note, section 4.7.1, has been improved. The receive buffer size has been increased to 4KB. As a result, the FT90x Revision C can hold two maximum-size packets at the same time to avoid packet loss.

4.8 SPI

Introduction:

The SPI in FT90x Revision C is similar to the SPI in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

A set of registers have been added to provide extra functions:

- SPCR2: Additional controls register to configure the SPI clock speed, data order and check RX FIFO status.
- SPSR2: Additional statuses register to check the TX and RX FIFO status.
- SFCR2: Additional FIFO control register to configure the TX and RX FIFO trigger level.
- TFER: New register to indicate the TX FIFO level, similar to RX_FIFO_COUNT for RX FIFO.
- BAUD: New register to configure the SPI clock speed

For more information regarding the new registers, please refer to BRT_AN_020_FT90x_Revison_C_User_Manual.

4.9 UART

Introduction:

The UART in FT90x Revision C is similar to the UART in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

- XON is issued when the level of the RX buffer is less than the lower trigger level.
- Receiving data which matches XOFF2 is written in the RX buffer.
- In 9-bit data mode, an interrupt is asserted when the receiving data matches special character 4 (bit 8 UART_NMR[5], bit 7..0 in XOFF2). A matching XOFF2 does not trigger an interrupt if the UART is in 9-bit data mode if the 9-th bit (UART_NMR[5]) does not match.

4.10 USB Peripheral

Introduction:

The USB Peripheral Controller in FT90x Revision C is similar to the USB Peripheral Controller in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

- The total buffer size to be shared by endpoint 1 to 7 is 6kB (endpoint 0 has its own 64-byte memory). One of the data endpoints (EP1-7) can be configured as a High Bandwidth Isochronous IN endpoint. For more information on the High Bandwidth Isochronous endpoint, please refer to BRT_AN_020_FT90x_Revison_C_User_Manual.
- A bit (NYET) is added to choose when the NYET packet is sent. Set to "1", the USB Peripheral Controller will not send NYET if it has a secondary buffer available. Otherwise, it will send NYET regardless of whether the secondary buffer is available or not.
- A bit (CONT_RW) is added to eliminate the wait-cycle on the CPU bus when it does stream in/stream out from/to the USB Peripheral memory. Otherwise, every write/read to the USB Peripheral memory will be followed by a wait-cycle. It is a performance improvement over the FT900 Revision B.

4.11 USB Host

Introduction:

The USB Host Controller in FT90x Revision C is similar to the USB Host Controller in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The issues described in TN_159 FT90x Errata Technical Note, section 4.8, have been fixed. A new bit (PSWN) has been added. When OC_DETECT_EN is set and an over current condition occurs, hardware will automatically set this bit. This bit cannot be cleared by SW as long as an OC condition exists. When this bit is set, external VBUS is disabled.

4.12 Watchdog

Introduction:

The Watchdog in FT90x Revision C is similar to the Watchdog in FT90x Revision B with some improvements as stated below.

Change in FT90x Revision C:

The behavior when a watchdog timeout occurs has been changed. The first time the timeout occurs, a special interrupt is generated and the CPU will jump to address 4. This interrupt must be cleared; otherwise subsequent first roll-over will not trigger further interrupt. If the watchdog timer is not cleared in time, and a second timeout occurs, there will be a global reset generated that will behave like a POR with a register bit set to indicate that the reset is caused by the watchdog's second roll-over.

5 PCB Design suggestions to retain compatibility with both revisions

The FT90x Revision C chips have 3 pins which require different voltages compared to Revision B, namely FSOURCE, VPP and VBAT. This section suggests an approach to board design so that both Revision B and C chips can be used.

5.1 FSOURCE and VPP

FSOURCE and VPP in FT90x Revision C are re-named as VCC1V2 and VCCIO3V3 to indicate their voltage requirement (refer to the FT900/1/2/3 and FT905/6/7/8 Revision C datasheets, which can be accessed via Appendix A below). These requirements differ from Revision B, so a PCB that supports both revisions must take care to provide to correct voltages to the currently used IC. A suggestion is as follows:

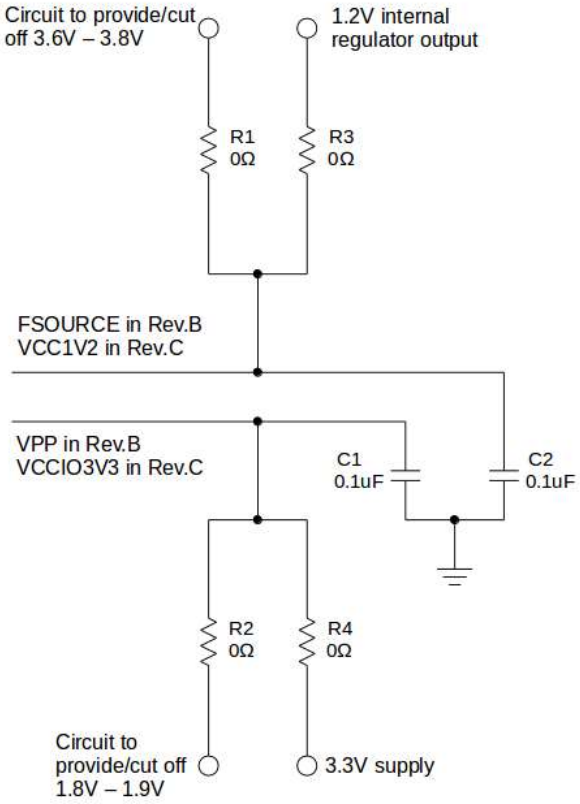

Figure 5.1 – Power Circuit Suggestion for Compatibility with Revision B and C

When Revision B is used, leave R3, R4, C1 and C2 unconnected. When Revision C is used, leave R1 and R2 unconnected. Note that if EFUSE programming is not required in Revision B, FSOURCE and VPP should be floating, which means R1 and R2 are not needed as well.

5.2 VBAT

In Revision B, the VBAT pin is not bonded out. As a result, a Revision B chip can be connected to the same 1.5V battery supply meant for Revision C without affecting the operation of the chip.

6 Contact Information

Headquarters – Singapore

Bridgetek Pte Ltd
178 Paya Lebar Road, #07-03
Singapore 409030
Tel: +65 6547 4827
Fax: +65 6841 6071

E-mail (Sales) sales.apac@brtchip.com
E-mail (Support) support.apac@brtchip.com

Branch Office – Taipei, Taiwan

Bridgetek Pte Ltd, Taiwan Branch
2 Floor, No. 516, Sec. 1, Nei Hu Road, Nei Hu District
Taipei 114
Taiwan, R.O.C.
Tel: +886 (2) 8797 1330
Fax: +886 (2) 8751 9737

E-mail (Sales) sales.apac@brtchip.com
E-mail (Support) support.apac@brtchip.com

Branch Office - Glasgow, United Kingdom

Bridgetek Pte Ltd.
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales.emea@brtichip.com
E-mail (Support) support.emea@brtchip.com

Branch Office – Vietnam

Bridgetek VietNam Company Limited
Lutaco Tower Building, 5th Floor, 173A Nguyen Van Troi,
Ward 11, Phu Nhuan District,
Ho Chi Minh City, Vietnam
Tel : 08 38453222
Fax : 08 38455222

E-mail (Sales) sales.apac@brtchip.com
E-mail (Support) support.apac@brtchip.com

Web Site

http://brtchip.com/

Distributor and Sales Representatives
Please visit the Sales Network page of the Bridgetek Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

FT90x Product Page

AN_324 FT900 User Manual

BRT_AN_020_FT90x_Revison_C_User_Manual

TN_159 FT90x Errata Technical Note

FT900/FT901/FT902/FT903 Datasheet

FT905/FT906/FT907/FT908 Datasheet

FT900/FT901/FT902/FT903 Revision C Datasheet

FT905/FT906/FT907/FT908 Revision C Datasheet

Acronyms and Abbreviations

Terms	Description
ADC	Analogue to Digital Converter
CAN	Controller Area Network
DAC	Digital to Analogue Converter
FIFO	First In First Out
NC	No Connection
PWM	Pulse Width Modulation
RTC	Real-time Clock
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

List of Tables

Table 2.1 - Change Summary 5
Table 2.2 - FT90x Revision B Part Numbers 5
Table 2.3 - FT90x Revision C Part Numbers 5

List of Figures

Figure 5.1 – Power Circuit Suggestion for Compatibility with Revision B and C 12

Appendix C – Revision History

Document Title: BRT_AN_019 FT90x Revision B to Revision C - Migration Guide

Document Reference No.: BRT_000171

Clearance No.: BRT#088

Product Page: http://brtchip.com/ft900/

Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	2017-08-02
1.1	Added PCB design suggestion for compatibility with both Rev.B and Rev.C. Added part numbers for both Rev.B and Rev.C	2017-11-01