Application Note

AN_304

FT90x Microcontroller Benchmark

Version 1.1

Issue Date: 2015-07-18

Application note to compare the performance of the FT90x to typical microcontrollers.

Use of FTDI devices in life support and/or safety applications is entirely at the user’s risk, and the user agrees to defend, indemnify and hold FTDI harmless from any and all damages, claims, suits or expense resulting from such use.
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1 Introduction

In microcontroller data sheets, DMIPS are quoted to compare the performance of the device. This application note explains DMIPS and highlights the speed of FTDI’s FT90x microcontroller.

1.1 Overview

1.1.1 Dhrystone Source code

Dhrystone is a computer program that calculates the millions of instructions handled per second (MIPS) based on a standardized Dhrystone application. The source code is freely available throughout the internet. The version used in the Application Note is available from this link [Dhrystone-2.1.tar.gz](Dhrystone-2.1.tar.gz).

1.1.2 Dhrystone explanation

Dhrystone MIPS (DMIPS) allow you to compare processors that have different instruction sets. While two processors may have the same MIPS (how many instructions they can execute in a second - basically clock speed), it can take the two processors a different number of instructions to complete the same calculation or task because they have different instruction sets. So DMIPS measures not just instructions per second but gives an idea of how long overall it will take one processor to perform a task versus another, taking into account the different number and kinds of instructions the processors will have to use to complete the task. Because of this, DMIPS can't just be calculated from MIPS, you have to actually measure them using the Dhrystone benchmark testing. And this is also why DMIPS can be greater than 1 DMIPS/MHZ - due to a particular instruction set, 1 instruction can actually be getting more done than 1 instruction on another processor. For example 16 bit architecture is likely to be more efficient than an 8-bit one for some tasks.

1.1.3 FT90x

The FT90x is a complete System-On-Chip 32-bit RISC microcontroller for embedded applications featuring high performance and a full feature set for system connectivity enabling a high level of functional integration.

The full datasheet of the FT90x device is available to download from [FTDI Chip](FTDI Chip).

Table
1.2 Comparison Table

<table>
<thead>
<tr>
<th>Microcontroller / Core</th>
<th>Bus (bits)</th>
<th>DMIPS/MHz</th>
<th>Maximum frequency (MHz)</th>
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<tbody>
<tr>
<td>FT90x / FT32</td>
<td>32</td>
<td>3.1</td>
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<td>RX600</td>
<td>32</td>
<td>1.65</td>
<td>100</td>
</tr>
<tr>
<td>AVR32</td>
<td>32</td>
<td>1.38</td>
<td>66</td>
</tr>
<tr>
<td>Pic 24</td>
<td>16</td>
<td>0.5</td>
<td>80</td>
</tr>
<tr>
<td>MSP430</td>
<td>16</td>
<td>0.3</td>
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<td>Arm Cortex-A9</td>
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<td>2</td>
<td>1000</td>
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<td>Arm Cortex-A5</td>
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<td>1000</td>
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<td>Synopsys ARC EM6</td>
<td>32</td>
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<td>420</td>
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</table>

Table 1.1 MCU Comparison Table

1.3 Comparison Graph

![Graph showing comparison of different microcontrollers' performance](image-url)
1.4 Summary

Many commercial MCU’s display the DMIPS/MHz as per the Table 1.1 however, these figures are based on 0 wait state operation. Many Flash based MCU’s usually max out 0WS at around 25MHz to 30MHz, so for operation beyond that you have to add 1, 2 or 3 wait states to run the MCU at its maximum stated operating frequency and this limitation is in general not widely publicised. Adding wait states, especially to a RISC CPU cripples the performance. FTDI’s shadow RAM architecture overcomes this limitation by executing out of shadow RAM at true 0 WS up to the full operating core frequency of the MCU (100MHz), without compromise.
2 Contact Information

Head Office – Glasgow, UK
Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA
Future Technology Devices International Limited
(USA)
7130 SW Fir Loop
Tigard, OR 97223-8160
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan
Future Technology Devices International Limited
(Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales@ftdichip.com
E-mail (Support) tw.support@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China
Future Technology Devices International Limited
(China)
Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site
http://ftdichip.com

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Appendix A – References

Document References
DS_FT900Q – FT900 Datasheet

Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Terms</th>
<th>Description</th>
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<tbody>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DMIPS</td>
<td>Dhrystone Million Instructions Per Second</td>
</tr>
<tr>
<td>MCU</td>
<td>Microcontroller</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computing</td>
</tr>
<tr>
<td>WS</td>
<td>Wait States</td>
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</table>
Appendix B – List of Tables & Figures

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Figure 1.1 MCU Comparison Graph
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<th>Revision</th>
<th>Changes</th>
<th>Date</th>
</tr>
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<tbody>
<tr>
<td>1.0</td>
<td>First release</td>
<td>2014-03-13</td>
</tr>
<tr>
<td>1.1</td>
<td>Update to performance figures</td>
<td>2015-07-13</td>
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