Application Note

BRT_AN_097

Selection and Integration of LVDS LCD Panels with VM820C

Version 1.0

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Guide to Selecting and Integrating LVDS Panels with the VM820C Development Module.

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1 Introduction

Several interface standards are commonly used for communication with TFT LCD panels, including:

i. Parallel Interface-(RGB)
ii. Low Voltage Differential Signaling (LVDS)
iii. Mobile Industry Processor Interface (MIPI-DSI)
iv. High-Definition Multimedia Interface (HDMI)
v. Embedded DisplayPort (eDP)

Among these, LVDS (Low Voltage Differential Signaling) stands out as a widely adopted interface in display technologies due to its high-speed performance and low power consumption. It transmits digital data over differential pairs—each comprising a positive and a negative signal line—using a low voltage differential swing, typically between 250–450 mV. This differential signaling minimizes electromagnetic interference (EMI) and enhances signal integrity, making it ideal for high-resolution display applications with data rates reaching several gigabits per second.

Bridgetek has traditionally provided Embedded Video Engine (EVE) graphic controller ICs, such as the BT81X and BT88X series, which utilize the RGB parallel interface. With the introduction of the BT820B, Bridgetek expands its EVE portfolio to support LVDS connectivity for TFT LCD panels, marking a significant advancement in display interface capability.

The VM820C module integrates the BT820B EVE IC into a compact, credit card–sized development platform. It features both LVDS receiver and transmitter functions, enabling the module to interface with LVDS input sources (e.g., cameras) and drive high-resolution LVDS LCD panels.

This application note provides detailed guidance on the selection, interfacing, and operation of LVDS LCD panels in conjunction with the VM820C development module, supporting designers in successful evaluation and integration of these technologies.

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2 Selecting and purchasing LVDS LCD Panels

2.1 Types of LVDS Panels Supported

LVDS display panels are high-resolution TFT screens widely used in premium electronic products. The VM820C development module supports these panels via LVDS interfaces that offer both single-channel and dual-channel configurations, each utilizing four data lanes.

The single-channel mode supports resolutions up to 1366 × 768 @ 60 Hz. For higher resolutions, the dual-channel mode is required, enabling support for resolutions up to 1920 × 1200 @ 60 Hz. It is important to note that dual-channel mode cannot be used to drive two separate single-channel displays. Table 1 outlines common LVDS panel resolutions and their corresponding channel requirements.

Resolution	Channel
1920 * 1200	Dual
1920 * 1080	Dual
1920 * 720	Dual
1280 * 800	Single
1024 * 768	Single
1024 * 600	Single
800 * 600	Single
800 * 480	Single
640 * 480	Single

Table 1 - Common LVDS Panel Resolutions

2.2 LVDS Panel Selection

Before selecting an LVDS panel, system developers are strongly advised to first identify the key requirements of their application—such as display size, resolution, and touch functionality.
The following criteria should be carefully considered when evaluating and selecting a suitable LVDS panel:

Display Size and Format

- Diagonal Size (e.g., 10.1", 15.6")
- Aspect Ratio (e.g., 16:9, 4:3)
- Active Area Dimensions (e.g., 344.16 mm × 193.59 mm)

Resolution

- Pixel Resolution (e.g., 1280×800, 1920×1080)
- Pixel Pitch (distance between adjacent pixels)

Interface Type

- LVDS Channel Configuration
  - Single-channel, dual-channel
  - Each channel supports up to 24 bits (8 bits per RGB)

- Signal Mapping / Bit Mapping
  - JEIDA or VESA standard
  - Color Depth: 6-bit or 8-bit

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Backlight Configuration

- LED Backlight Type: edge-lit or direct-lit
- Connector Type and Pinout
- Brightness (in cd/m²)
- Backlight Driver Requirement: external or integrated

Touch Panel Integration (if applicable)

- Touch Type: resistive, capacitive.
- Touch Interface: I²C

For recommended LCD panels, please contact Bridgetek sales.

2.3 BT820B-Compatible LVDS Panel Types

Table 2 provides a list of display panel models featuring a range of resolutions and interface formats that have been tested and validated for reliable operation with the BT820B EVE graphics controller. As LVDS panels typically adhere to standardized signaling conventions, they offer robust performance and are generally free from compatibility issues, provided that the format, resolution, timing parameters, and voltage levels are correctly matched.

Resolution	Chann	RGB	Standard
1920 * 1200	Dual	8	VESA
1920 * 720	Dual	8	VESA
1440 * 540	Single	8	VESA
1280 * 800	Single	8	VESA
1280 * 800	Single	6	JEIDA
1024 * 600	Single	6	JEIDA
800 * 600	Single	8	JEIDA

Table 2 - Types of LVDS LCD Panel Validated

2.4 BT820B-verified LVDS-HDMI Converter Boards

In addition to supporting LVDS LCD panels, the VM820C development board can interface with LVDS-to-HDMI converter boards, offering a convenient and flexible solution for evaluating the BT820B, particularly during early development stages. While the BT820B EVE graphics controller is designed to interface with LVDS-based TFT panels, suitable high-resolution LVDS panels may not always be readily available or cost-effective for quick prototyping and testing.

By incorporating an LVDS-to-HDMI adapter, developers can take advantage of widely available HDMI-compatible displays—such as computer monitors, televisions, or projectors—to evaluate the full graphical capabilities of the BT820B without being constrained to a specific LVDS panel. Most importantly, these adapters allow the BT820B to demonstrate its ability to drive various resolutions, including:

- Standard resolutions such as 800 × 600 (SVGA), 1024 × 768 (WSVGA) and 1280 × 800 (WXGA)
- High resolutions up to 1920 × 1080 (FHD) in dual-channel LVDS mode

This enables comprehensive testing of the controller's video output, signal integrity, and timing configuration across different display sizes and aspect ratios. It also streamlines the debugging process by using familiar HDMI test equipment and readily accessible monitors.

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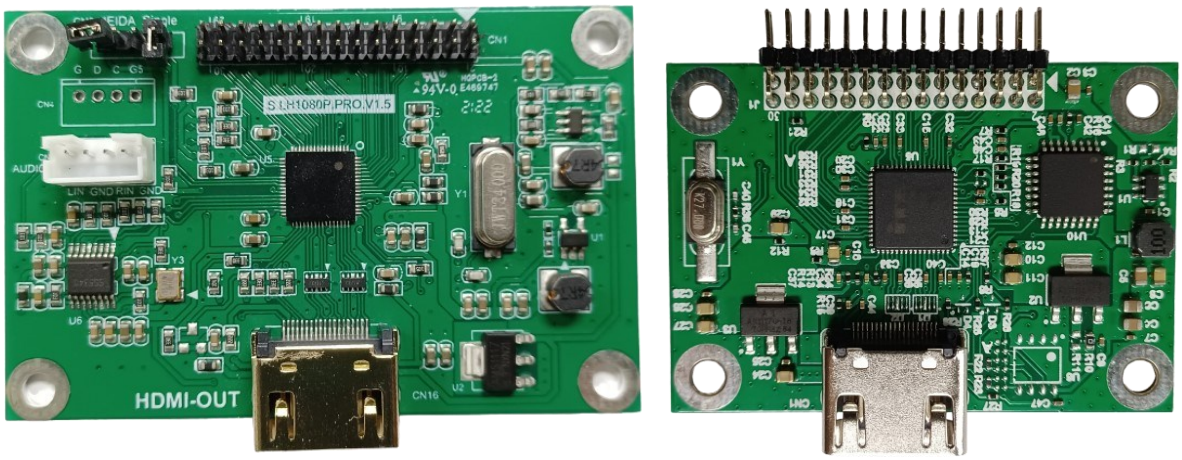
Overall, LVDS-to-HDMI adapters serve as an effective bridge during development, helping engineers validate display output performance and resolution compatibility of the BT820B before committing to a final panel selection. However, these adapters do not support touch interface evaluation, which must be connected and tested separately as outlined in Section 3.2.

Table 3 lists two LVDS-to-HDMI converter boards that have been tested and confirmed to work reliably with the BT820B.

Figure 1 provides images of these tested boards.

Manufacturer Part No.	Manufacturer
SLH1080P_PRO V1.5	Guangzhou Seenku Technology CO. LTD
S.LH1080P.AUDIO.V20	Unbranded

Table 3 - Tested and Verified LVDS to HDMI Converter



SLH1080P_PRO V1.5 **S.LH1080P.AUDIO.V20**

Figure 1 - LVDS to HDMI Convert Boards

2.5 LVDS-to-HDMI Converter Board Test Setup and Results

The following section presents the test setup using one of the listed LVDS-to-HDMI converter boards. Figure 2 illustrates the setup in which the 'SLH1080P_PRO V1.5' board converts LVDS transmission signals from the VM820C into HDMI signals, which are then displayed on an HDMI monitor.

Note that the required supply voltage for the adapter board may vary. In this case, the board requires a +5V DC supply, whereas the default voltage at the header is 3.3V. Users will need to rewire the power connections to draw +5V directly from the VM820C's power input connector.

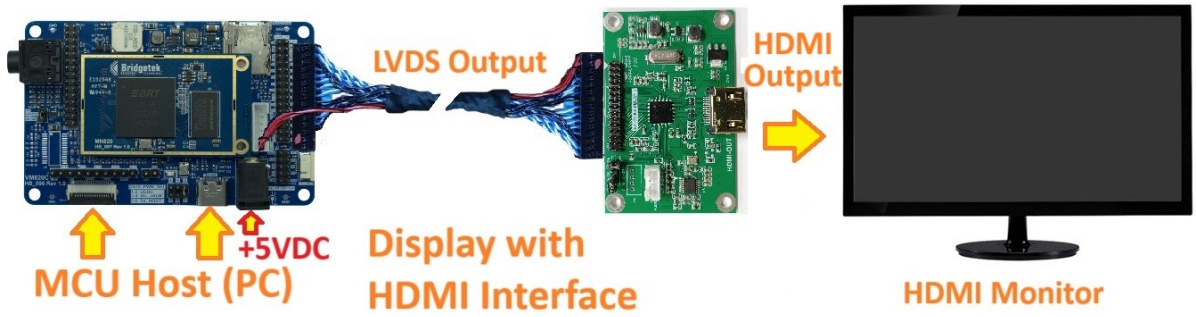


Figure 2 - LVDS-to-HDMI Converter Board Test Setup

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Refer to Table 4 - Tested Output Resolution for the output resolutions @ 60Hz with respect to BT820B register configuration settings tested with a VM820C board using the 'SLH1080P_PRO V1.5' converter board. The results cover both JEIDA and VESA formats.

Resolution		Channel	SO_MODE	TXCLKDIV	PCLK (MHz)	HSYNC1	VSYNC1	HOFFSET	VOFFSET	HCYCLE	VCYCLE
W	H										
1920	1080	2	3	3	72	20	4	220	28	2140	1108
1600	900	2	3	5	57.6	20	4	32	68	1632	968
1440	900	2	3	5	57.6	20	4	240	40	1680	940
1280	1024	2	3	6	41.14	20	4	52	4	1332	1028
1280	800	1	0	3	72	20	4	156	36	1436	836
1280	720	1	0	3	72	20	4	200	80	1480	800
1024	768	1	0	4	57.6	20	4	180	20	1204	788
800	600	1	0	6	41.14	20	4	220	76	1020	676

Table 4 - Tested Output Resolutions

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3 Connecting LVDS Panels and Adapters to VM820C

The VM820C board is equipped with two LVDS transmit channels, channel 0 (Tx0) and channel 1 (Tx1), each consisting of four data lanes for delivering video data to an external display panel. The Tx0 channel transmits odd-bit data, while the Tx1 channel transmits even-bit data.

This section provides developers with guidance on interfacing their selected LCD panels with the BT820B via the VM820C platform. It outlines the necessary connections for signal transmission, backlight control and touch sensing functionality.

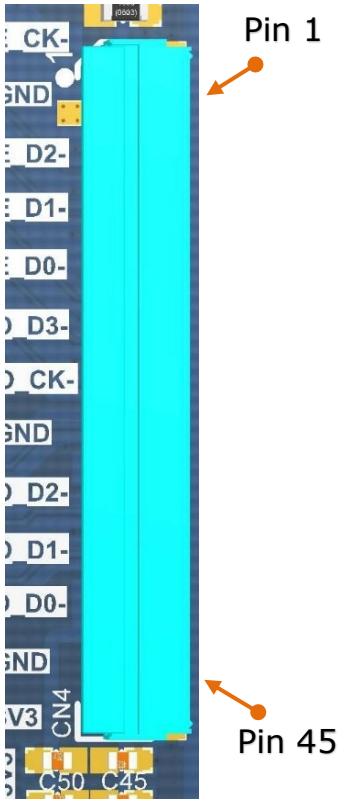
3.1 LVDS Transmit Signal Connection

The VM820C offers two connector options for interfacing with LVDS LCD panels:

- 45 positions – 0.5mm pitch FPC connector
- 30 positions – dual row, 2mm pitch header

3.1.1 45-Position FPC Connector Pin Definition

Figure 3 shows the pinout of connector CN4, a 45-position, 0.5 mm pitch FPC connector from Hirose (part number: FH34SRJ-45S-0.5SH (50)). The connector features a dual-contact design, enabling connections on both the top and bottom surfaces of the connector. Due to this, care must be taken to ensure correct FPC (Flexible Printed Circuit) cable orientation during installation to avoid reverse connections.



Pin No.	Name
1	LEDK
2	LEDK
3	LEDA
4	LEDA
5	NC
6	GND
7	LVDS_TX1_D3_P
8	LVDS_TX1_D3_N
9	GND
10	LVDS_TX1_D2_P
11	LVDS_TX1_D2_N
12	GND
13	LVDS_TX1_CLK_P
14	LVDS_TX1_CLK_N
15	GND
16	LVDS_TX1_D1_P
17	LVDS_TX1_D1_N
18	GND
19	LVDS_TX1_D0_P
20	LVDS_TX1_D0_N
21	GND
22	LVDS_TX0_D3_P
23	LVDS_TX0_D3_N
24	GND
25	LVDS_TX0_D2_P
26	LVDS_TX0_D2_N
27	GND
28	LVDS_TX0_CLK_P
29	LVDS_TX0_CLK_N
30	GND
31	LVDS_TX0_D1_P
32	LVDS_TX0_D1_N
33	GND
34	LVDS_TX0_D0_P
35	LVDS_TX0_D0_N
36	GND
37	NC
38	NC
39	NC
40	NC
41	VCC3V3
42	VCC3V3
43	VCC3V3
44	VCC3V3
45	VCC3V3

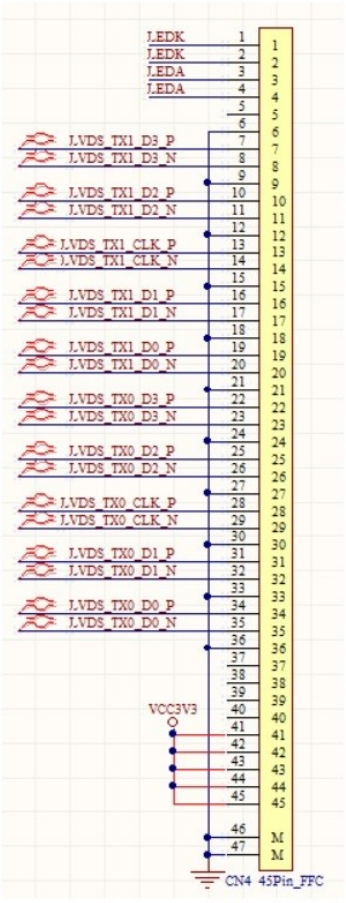


Figure 3 - LVDS Transmit Connector: 45 Position FPC Pin Definition

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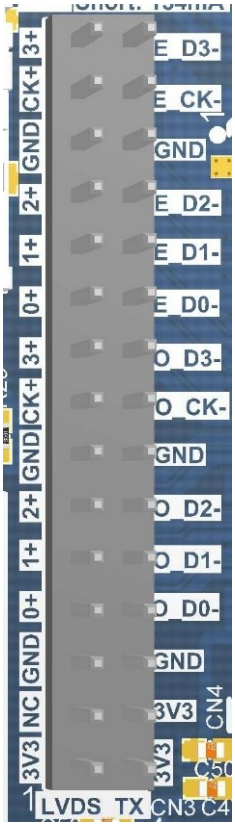
3.1.2 30-Position Header Pin Definition

Figure 4 illustrates the pinout for CN3, a 30-position, 2mm pitch dual-row header. This connector follows standard industrial pin assignments commonly used on LVDS-to-HDMI converter boards. Since these boards usually do not require backlight control, the header does not provide LED+ or LED– lines.

CN3 is designed to support interfacing with:

i. LVDS LCD Panels
ii. LVDS to HDMI converter boards



Pin No.	Name
1	VCC3V3
2	VCC3V3
3	NC
4	VCC3V3
5	GND
6	GND
7	LVDS_TX0_D0_P
8	LVDS_TX0_D0_N
9	LVDS_TX0_D1_P
10	LVDS_TX0_D1_N
11	LVDS_TX0_D2_P
12	LVDS_TX0_D2_N
13	GND
14	GND
15	LVDS_TX0_CLK_P
16	LVDS_TX0_CLK_N
17	LVDS_TX0_D3_P
18	LVDS_TX0_D3_N
19	LVDS_TX1_D0_P
20	LVDS_TX1_D0_N
21	LVDS_TX1_D1_P
22	LVDS_TX1_D1_N
23	LVDS_TX1_D2_P
24	LVDS_TX1_D2_N
25	GND
26	GND
27	LVDS_TX1_CLK_P
28	LVDS_TX1_CLK_N
29	LVDS_TX1_D3_P
30	LVDS_TX1_D3_N

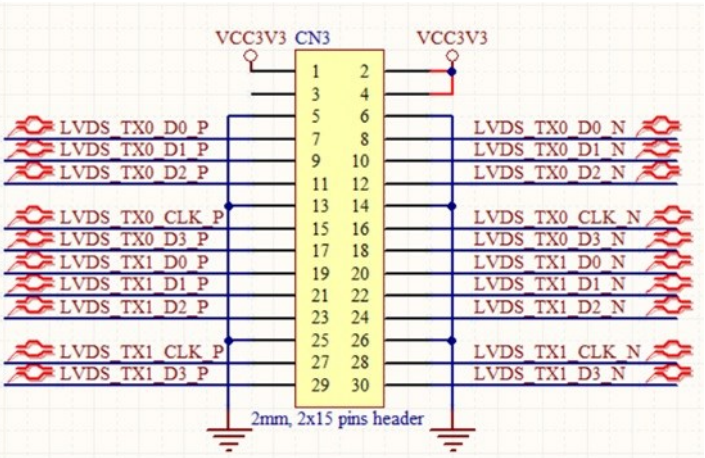


Figure 4 - LVDS Transmit Connector: 30 Position Header Pin Definition

3.1.2.1 Interfacing with LVDS LCD Panels

The CN3 header is intended for use with LVDS cable assemblies rather than FPC cables. Unlike FPC cables, which have fixed pin configurations, LVDS cables allow individual wire rearrangement—offering greater flexibility when adapting to the varying pinouts of different LCD panels or converter board.

3.1.2.2 Interfacing with LVDS to HDMI Converter Boards

LVDS-to-HDMI converter boards commonly utilize 30-position headers to receive LVDS video signals. While there is no formal standard for these pinouts, a widely adopted de facto standard is used by many manufacturers—and the 30-position header on the VM820C is designed to match this convention.

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3.2 Connecting LCD Panels and Converter Boards to VM820C

This section explains how designers can utilize the onboard connectors and headers to integrate external LVDS LCD panels and converter boards with the VM820C evaluation module.

3.2.1 Connecting LVDS LCD Panels to VM820C via 45 pos FPC connector

The 45-position FPC connector on the VM820C is intended to demonstrate the BT820B's capability to support dual-channel LVDS panels with resolutions up to 1920×1200. This interface is commonly used with 10-inch class LCD panels typically found in portable tablet devices.

Unlike discrete wire headers, FPC connectors have fixed pin assignments that cannot be reconfigured. However, many 45-pin LVDS LCD panels conform to a widely adopted industry-standard pinout. Table 5 below illustrates the two most common 45-pin configurations.

Pin No.	Pin Assignment	
	Configuration 1	Configuration 2
1	LEDK	NC
2	LEDK	NC
3	LEDA	NC
4	LEDA	NC
5	NC	NC
6	GND	GND
7	E_3+	E_3+
8	E_3-	E_3-
9	GND	GND
10	E_2+	E_2+
11	E_2-	E_2-
12	GND	GND
13	E_CLK+	E_CLK+
14	E_CLK-	E_CLK-
15	GND	GND
16	E_1+	E_1+
17	E_1-	E_1-
18	GND	GND
19	E_0+	E_0+
20	E_0-	E_0-
21	GND	GND
22	O_3+	O_3+
23	O_3-	O_3-
24	GND	GND
25	O_2+	O_2+
26	O_2-	O_2-
27	GND	GND
28	O_CLK+	O_CLK+
29	O_CLK-	O_CLK-
30	GND	GND
31	O_1+	O_1+
32	O_1-	O_1-
33	GND	GND
34	O_0+	O_0+
35	O_0-	O_0-
36	GND	GND
37	NC	NC
38	NC	NC
39	NC	NC
40	NC	GND
41	VDD	VDD
42	VDD	VDD
43	VDD	VDD
44	VDD	VDD
45	VDD	VDD

Table 5 - Common 45 Position LVDS Panel Pin Definition

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The VM820C's 45-position FPC connector aligns with **Configuration 1**, allowing for direct connection to compatible panels using standard FPC flex cables.

For panels following **Configuration 2**, where pins 1 through 4 are designated as No Connect (NC), designers should disable the onboard backlight driver to prevent high voltage application to LEDA/K. However, please note that even with the driver disabled, module supply voltage is still present on LEDA. Therefore, it is important to verify with the LCD manufacturer whether the panel can safely tolerate voltage on these NC-designated pins.

3.2.2 Connecting LVDS LCD Panels to VM820C via 30 pos header

When connecting LCD panels to the VM820C via the 30-position header, LVDS cables are used instead of FPC cables. These cables consist of multiple twisted wire pairs and are specifically designed to transmit high-speed digital signals with low power consumption and minimal electromagnetic interference (EMI).

LVDS cables are available in various forms, featuring different housing types and plug connectors to suit specific application needs. Figure 5 shows examples of commonly available LVDS cables.

Figure 5 - LVDS Cables

A key advantage of LVDS cables is their wiring flexibility, allowing users to rearrange individual wires to accommodate different pinouts. This makes them particularly suitable for interfacing with a wide range of LCD panels and LVDS converter boards.

LVDS LCD panels that use 30-position connectors are generally large, measuring more than 15 inches in size. These panels often require high-voltage inverters or LED backlight power supplies up to 50 V and may include multiple feedback channels for backlight regulation.

Since the VM820C does not include a high-power backlight driver, designers should use the CN7 power connector or an external power source to power the backlight drivers or inverters for these panels.

3.2.3 Connecting LVDS to HDMI Converter Boards to VM820C

Most LVDS-to-HDMI converter boards use a 30-position, dual-row, 2 mm pitch header to receive LVDS signals and power. To connect the VM820C to these converter boards, users can use an LVDS cable with dual-row 2 mm pitch housing on both ends, as illustrated in Figure 6.

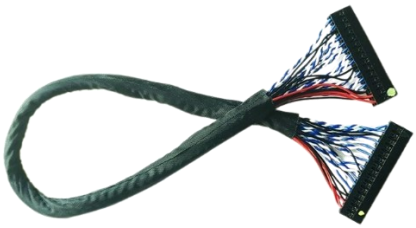

Figure 6 - Dual Row Housing LVDS Cable

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When using this header to drive an LVDS to HDMI converter board, ensure the converter board's power requirements are met. The header on VM820C supplies a fixed 3.3 V; if the converter board requires a different voltage, Power pins (red wires) with ground wires (black) can be detached from the housing and rewired to power connector CN7 or external power source.

If the converter board uses a non-standard header pinout, designers can reconfigure the LVDS cable connections to match the required assignment.

3.3 Touch Panel Interface

The BT820B controller supports I²C communication for Capacitive Touch Panels (CTP). These control signals are routed through the GPIO pins of the IC. Refer to Table 6 for the GPIO-to-controller signal mapping.

Pin	CTP-I2C	Type	Notes
GPIO8	RST_N	O	Reset to touch controller
GPIO7	INT_N	I	Interrupt from touch controller
GPIO6	SDA	IO	I2C data line
GPIO5	SCL	IO	I2C clock line.

Table 6 - Capacitive Touch Panels Interface

The VM820C offers two connector options for interfacing with touch panels:

- 6 positions - 0.5mm pitch FPC connector
- 10 positions –2x5, 2mm pitch header

3.3.1 6-Position FPC Connector Pin Definition

Figure 7 shows the pinout for the 6-position, 0.5 mm pitch bottom-contact FPC connector for interfacing to touch panels.

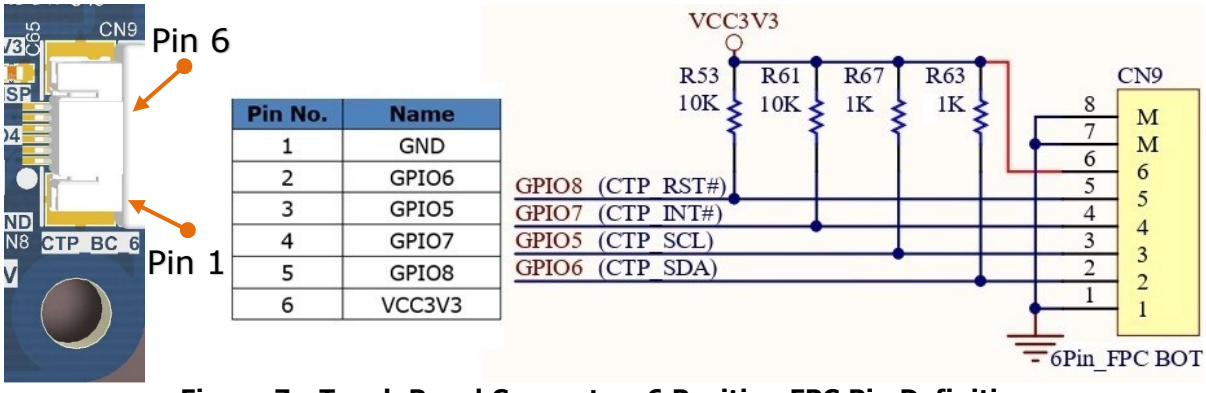

Figure 7 - Touch Panel Connector: 6 Position FPC Pin Definition

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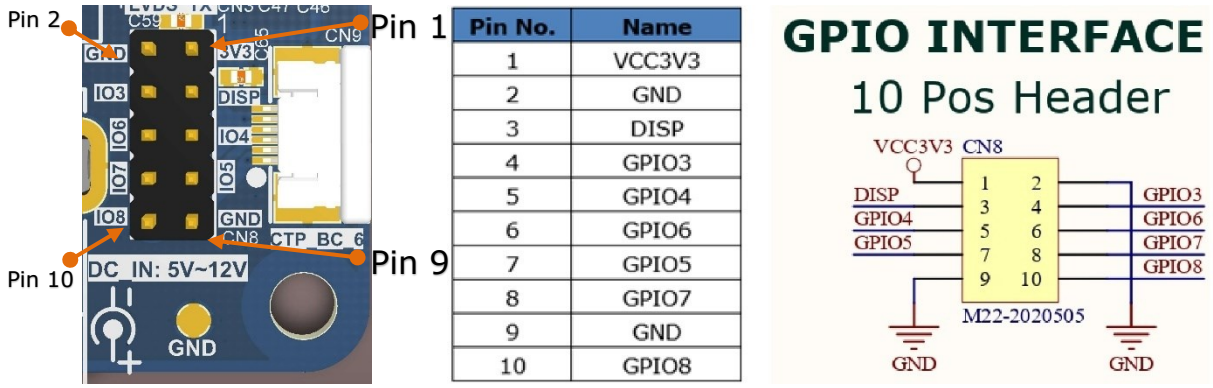
3.3.2 10-Position FPC Connector Pin Definition

The touch interface GPIOs are also accessible through a dual-row 10-position header, 2 mm pitch header, as illustrated in Figure 8.



Pin No.	Name
1	VCC3V3
2	GND
3	DISP
4	GPIO3
5	GPIO4
6	GPIO6
7	GPIO5
8	GPIO7
9	GND
10	GPIO8

Figure 8 - Touch Panel Connector: 10 Position Header Pin Definition

3.3.3 Connecting Capacitive Touch Panels to the VM820C

At present, there is no unified industry standard for capacitive touch panel connections. Typically, capacitive touch interfaces are provided via a flexible printed circuit (FPC) extending from the panel, terminated with exposed gold fingers for connection (refer to Figure 9). The FPC specifications—including length, pin count (commonly between 6 to 12 pins), pitch (typically 0.5 mm or 1.0 mm), and signal mapping — vary significantly among manufacturers.

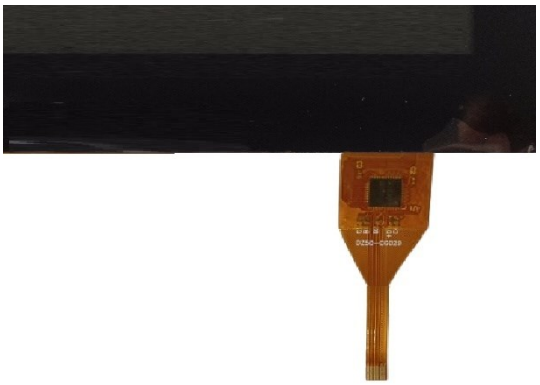


Figure 9 - Capacitive Panel Flexible PCB Interface

Due to this variability, it is often difficult to directly interface a capacitive touch panel with the VM820C module—particularly when also aligning with the corresponding LCD interface. Therefore, unless a custom-designed panel is selected, it is generally necessary to use an intermediate adapter board and additional wiring to complete the connection.

Several methods exist for achieving this connection. Two practical options are described below:

Option1: Connection via GPIO Header

In this method, the capacitive touch panel is connected to the VM820C's GPIO header through the use of two components:

1. FPC-to-2.54mm Header Adapter (matching CTP's flex PCB)
2. 2mm to 2.54mm Jumper Wires.

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Both components are readily available through global distributors and online suppliers. Purchase links are provided below for reference. Visual illustrations are provided in Figure 10 and Figure 11. Figure 12 demonstrates the complete setup.

FPC to 2.54mm Header Adapter – Suggested Sources:

- 6P-40P, 0.5mm 1mm FPC Adapter Board Ebay
- FPC ADAPT 40PIN 0.5 - 1MM (bare PCB only) Digikey
- FPC STICK 20PIN 0.5/1MM ADAPTER Digikey

2mm to 2.54mm Jumper Wire – Suggested Sources:

- 2.0mm to 2.54mm 40 PCs Ebay
- 2.0mm to 2.54mm Pitch Ribbon Cable - Ebay

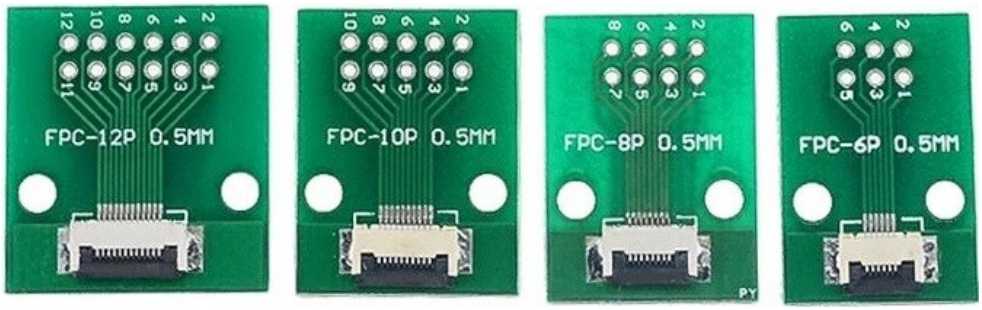

Figure 10 - FPC-to-2.54mm Header Adapter

Figure 11 - 2mm-to-2.54mm Jumper Wire

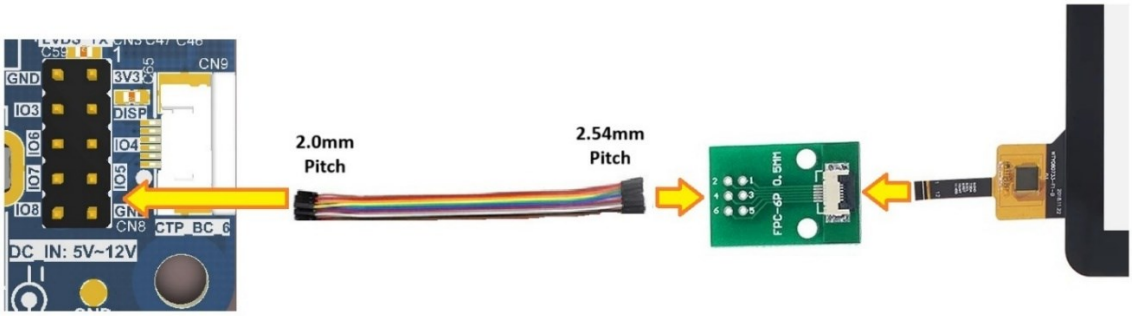

Figure 12 - Connecting CTP via Header

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Option 2: Connection via FPC connector

Alternatively, the capacitive touch panel can be connected to the VM820C using the onboard FPC connector, along with four components:

1. 6 position 0.5mm Pitch FPC-to-2.54mm Header Adapter (matching the VM820C's FPC connector)
2. FPC-to-2.54mm Header Adapter (matching CTP's flexible PCB)
3. 2.54mm Pitch Jumper Wires
4. 6 position 0.5mm Pitch FPC Cable

For components **1** and **2**, refer to Option 1 for illustrations and purchase links. Notably, the 2.54mm-to-2.54mm jumper wires used here are more commonly available than the 2.0mm-to-2.54mm wires. The 6-position FPC cable is also widely offered by multiple suppliers. Images and purchase links for components **3** and **4** are detailed below in Figure 13 and Figure 14 while Figure 15 demonstrates the setup.

2.54mm Jumper Wires – Suggested Sources:

- 2.54mm Jumper Wires - Ebay
- 2.54mm Jumper Wires - Digikey

6 position 0.5mm pitch FPC Cable – Suggested Sources:

- FPC Cables 4-40Pin 0.5mm pitch - Ebay
- CABLE FFC/FPC 6POS 0.5MM 1.18" - Digikey
- FPC Cable 6 Core - Element14

Figure 13 - 2.54mm Jumper Wire

Figure 14 - 6 Position 0.5mm FPC Cable

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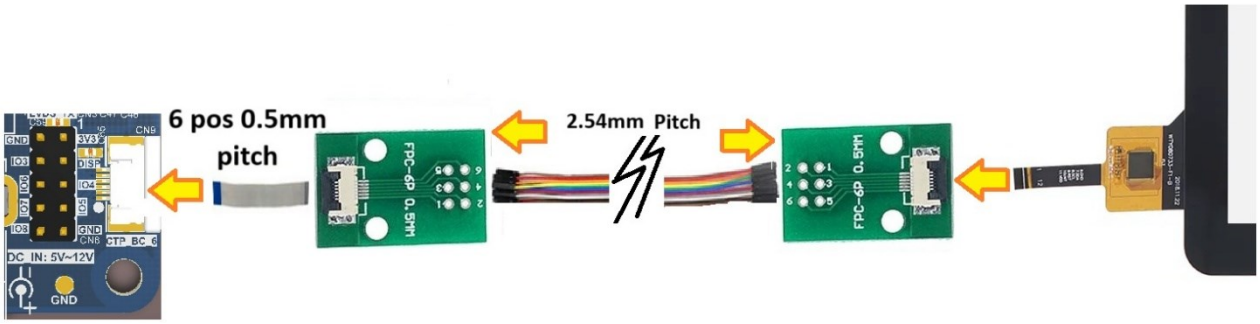

Figure 15 - Connecting CTP via FPC Connector

Additional Connection Considerations

When establishing the connection between the capacitive touch panel and the VM820C, please take note of the following:

- **Cable and Wire Lengths:**

  Jumper wires and FPC cables come in various lengths. It is recommended to choose lengths that align with the mechanical layout and simplify setup for the selected touch panel, while also keeping the total length within 0.5 meters to maintain signal integrity.

- **FPC Connector Types:**

  FPC connectors may come in top-contact, bottom-contact, or dual-contact configurations. Similarly, FPC cables may be forward-contact (contact fingers on the same side) or reverse-contact (contact fingers on opposite sides). It is important to ensure that the FPC cable matches the contact side of the connector installed on the VM820C module.

3.4 Driving LED Backlight

The VM820C evaluation board offers two methods for powering the LED backlight of connected LCD panels:

- **External Driver**: The input power (5 V to 12 V) is re-routed to a dedicated power connector, suitable for driving external LED drivers, such as those integrated within certain LCD panels.
- **Integrated Driver**: An onboard LED driver provides LED anode and cathode signals via the 45-position FPC connector.

3.4.1 External Driver via Power Connector

The VM820C can be powered via a 2.1 mm DC jack (CN11), accepting a DC input voltage in the range of 5 V to 12 V. This input power is routed to a 6-position, 2 mm pitch JST header (CN7), as shown in Figure 16, intended for powering external devices and LED drivers.

When using the DC jack to power the system, ensure that the power selection jumper on CN12 is set to Pins 3–4 to route power correctly to the VM820C.

In addition to power supply lines, the header includes a PWM signal, 'BKLIT_PWM', from the BT820B, enabling backlight brightness control through adjustable frequency (250 Hz to 10 kHz) and duty cycle. A 3.3 V pull-up signal is also available for enabling the LED driver, offering an always-on control option.

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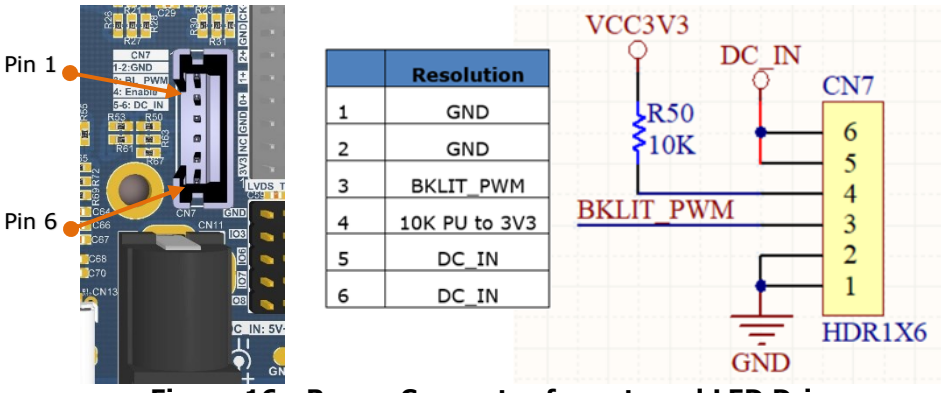

	Resolution
1	GND
2	GND
3	BKLIT_PWM
4	10K PU to 3V3
5	DC_IN
6	DC_IN

Figure 16 - Power Connector for external LED Drivers

3.4.2 Integrated Driver

The VM820C incorporates an onboard LED backlight driver circuit utilizing the Texas Instruments TPS61500. This driver is capable of powering up to four 3W LEDs with a 5 V input, or up to eight 3W LEDs when operating from a 12 V supply. The circuit implementation is illustrated in Figure 17.

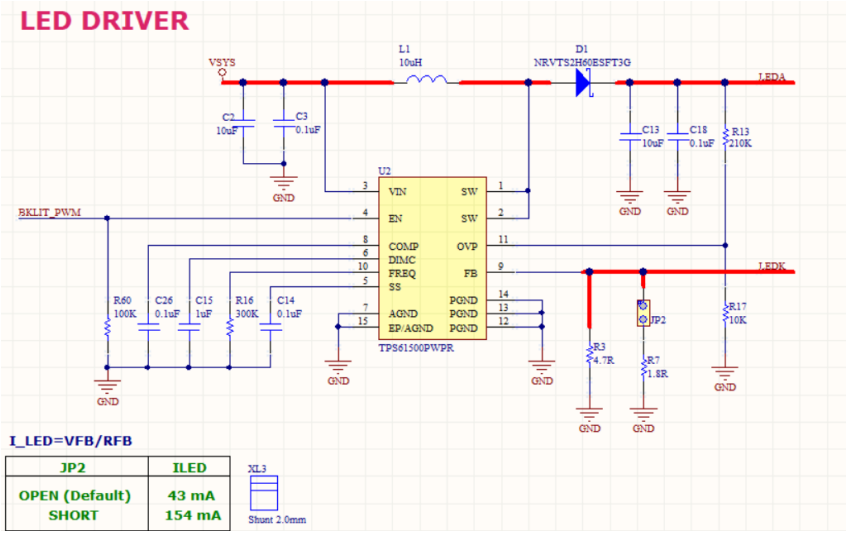

Figure 17 - Integrated LED Backlight Driver

The output of the LED driver is routed to the 45-position FPC connector for direct connection to LVDS LCD panels. The LED output current can be set to one of two fixed levels using jumper JP2:

- **43mA (JP2 open):** Optimized for a 5V power source (e.g., USB), ensuring adequate LCD backlight brightness while minimizing power draw.
- **154mA (JP2 shorted):** High-brightness mode designed for operation with a 12 V power supply; using lower input voltages may lead to circuit instability or unexpected system resets

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3.4.3 Configuring LED Driver's Output Current

Developers can configure the output current and Over-Voltage Protection (OVP) settings to accommodate the requirements of specific LCD panels or to attain desired brightness levels, as outlined in the following instructions.

LED Output Current Calculation:

The LED current can be adjusted by modifying the resistance at the driver's feedback (FB) pin. Use Equation 1 to calculate the total resistance R_T required to set the target current level:

$$I_{LED} = \frac{V_{FB}}{R_T}$$

Equation 1 - LED Driver ILED Calculation

Note: Voltage at feedback pin V_{FB} is regulated at 200mV.

After calculating total resistance R_T, implement the following changes:

- Replace **R3** with a resistor equal to the calculated $\mathbf{R_T}$.
- Remove jumper on JP2 eliminate the parallel resistance effect introduced by R7.

Refer to the Texas Instruments TPS61500 datasheet for detailed guidance and additional implementation considerations.

Modulating LED Backlight Brightness Using PWM

Once the LED current has been set, developers can further fine-tune the backlight brightness using the BT820B's PWM control signal, with two adjustment methods:

- **Frequency Adjustment:** Select a PWM frequency within the 250 Hz (lowest brightness) to 10 kHz (highest brightness) range.

- **Duty Cycle Adjustment:** Configure the duty cycle between 0–128, where 0 corresponds to the PWM signal being completely off, and 128 represents a fully on state.

For more information on configuring the PWM control signal, please consult the BT820B datasheet.

3.4.4 Configuring LED Driver's Over Voltage Protection

Over-Voltage Protection (OVP) is a critical safety and reliability feature integrated into LED backlight driver circuits. It protects the driver and associated components from damage due to excessive output voltage, particularly under abnormal or no-load conditions. The OVP threshold is typically set just above the maximum expected forward voltage of the connected LED array or LCD backlight.

LED Output Voltage Protection Calculation:

The OVP threshold of the VM820C's integrated backlight driver (TPS61500) can be adjusted by modifying the resistor values **R13** or **R17**, as illustrated in Figure 17. Use Equation 2Equation 2 - LED Driver OVP Calculation to determine the appropriate OVP setting based on the desired output voltage limit.

$$V_{ovp} = 1.229V \times \left(\frac{R13}{R17} + 1\right)$$

Equation 2 - LED Driver OVP Calculation

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4 Configuring BT820B for Optimal LVDS Panel Timing

4.1 Timing Parameters

The following section guides developers in understanding and adjusting the timing parameters of LVDS LCD panels when using the BT820B EVE IC.

Different LCD panels require different specific timing parameters, which developers must adjust based on the timing specifications requirement required by the panel manufacturer. Figure 18 below illustrates the LCD timing structure for displaying a single video frame.

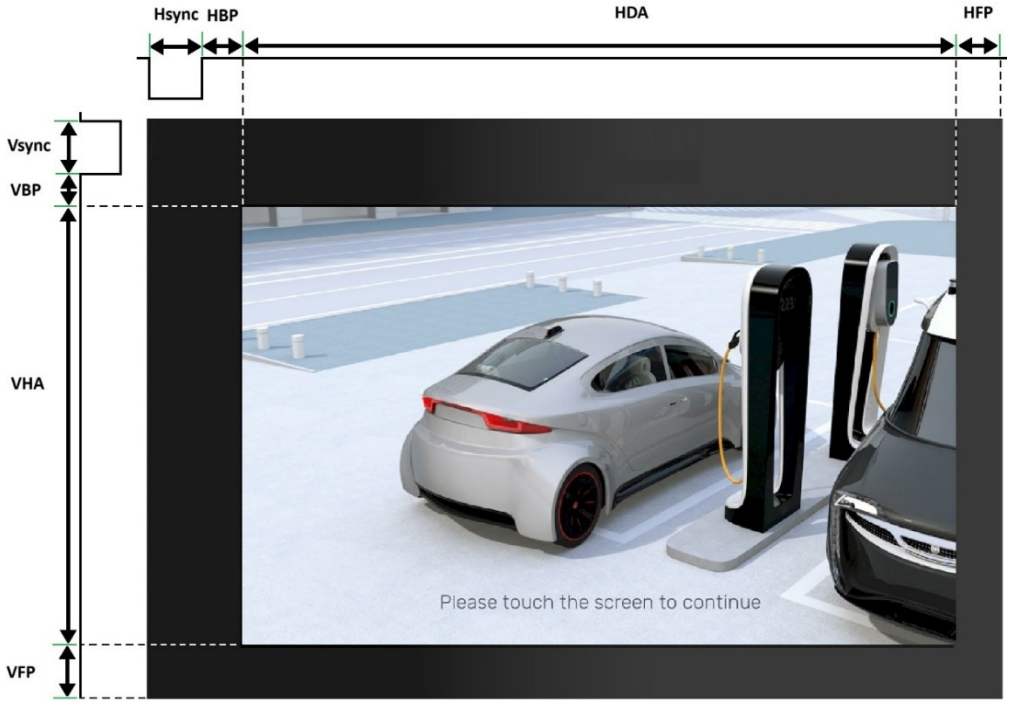

Figure 18 - LCD Timing During Frame Display

- **Hsync / Vsync: Horizontal Sync / Vertical Sync**

  Timing signals are used to synchronize the display refresh for each line (horizontal) and each frame (vertical). These pulses signal the start of a new line or frame.

- **HBP / VBP: Horizontal / Vertical Back Porch**

  The blanking time after the sync pulse and before the active display area begins. It's used to position the image correctly on screen.

- **HAD / VAD: Horizontal / Vertical Active Display Area**

  The part of the signal where actual image data is transmitted—what the user sees on the screen.

- **HFP / VFP: Horizontal /Vertical Front Porch**

  A brief interval of blanking time after the active display area and before the sync pulse. It helps ensure signal stability.

The following section illustrates how to configure the BT820B's output timing parameters to align with the requirements of LCD panels.

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4.2 Adjusting PCLK

In order to meet required frame rate (e.g. 60Hz) PCLK must be set to meet clock frequency requirement of selected LCD panel. The BT820B supports a programmable PCLK, up to 83.2MHz. To align the BT820B's LVDS_TX_PCLK output frequency with the required timing specifications, the PLL—which generates both the system clock and the pixel clock (PCLK)—must be configured accordingly. As shown in Table 7, which lists possible output clock values and their corresponding settings, developers can achieve the desired PCLK frequency by adjusting the 'TXCLKDIV' parameter. For a more detailed description of adjusting system and LVDS_TX_PCLK, please refer to BT820B datasheet and BT820B Programming Guide.

OSC (MHz)	SYSPLL_NS	Division Factor (TXCLKDIV+1)	LVDSTX PCLK (MHz)
38.4	15 (default)	4	72.00
		5	57.60
		6	48.00
		7	41.14
		8 (default)	36.00
	13	3	83.20
		4	62.40
		5	49.92
		6	41.60
		7	35.66

Table 7 - PCLK and LVDSTX Clock Configuration

To meet given reference specification operating PCLK frequency of 74.5MHz - 85MHz. We can set "SYSPLL.NS" out of default value to 13 and "TXCLKDIV" to 2 (setting "Division Factor" to 3) to generate PCLK of frequency 83.2MHz.

We can use the following formula to calculate **required PCLK frequency**:

PCLK (Hz)= Total Horizontal Pixels × Total Vertical Lines × Refresh Rate (Hz)
Where:

- Total Horizontal Pixels = HSYNC + HBP + HAD + HFP
- Total Vertical Lines = VSYNC + VBP + VAD + VFP
- Refresh Rate = typically 60 Hz (but can be 50, 75, etc.)

4.3 Adjusting Display Timing

This section outlines key timing parameters required for synchronizing display output with an LVDS panel. Proper configuration ensures stable image rendering and compliance with panel specifications.

4.3.1 Horizontal Timing Registers

BT820B horizontal timing registers define the line timings for visible pixels and non-visible pixels (blanking). For dual channel LVDS panel, the horizontal timing parameters listed in panel datasheet need to be doubled when calculating and filling into BT820B registers.

- **Horizontal Synchronization (REG_HSYNC0 and REG_HSYNC1):**

  Defines the duration of the horizontal synchronization signal. It marks the end of one horizontal line and the beginning of the next. REG_HSYNC0 = HFP, REG_ HSYNC1 = HFP + HSYNC.

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- **Horizontal Offset (REG_HOFFSET):**

  Horizontal offset defines the total number of non-visible pixels. REG_HOFFSET = HFP + HSYNC + HBP.

- **Horizontal Active Display Area (REG_HSIZE):**

  This is the region within each horizontal line where actual pixel data is transmitted. It defines the horizontal resolution of the panel. REG_HSIZE = HAD.

- **Horizontal Cycle (REG_HCYCLE):**

  Horizontal cycle defines the total number of pixels (visible and non-visible) per line. REG_HCYCLE = HSYNC + HBP + HAD + HFP.

4.3.2 Vertical Timing Registers

- **Vertical Synchronization (REG_VSYNC0 and REG_VSYNC1):**

  The vertical synchronization pulse signals the start of a new frame. It resets the scan from the bottom of the screen back to the top. The required width is typically defined in terms of lines. REG_VSYNC0 = VFP, REG_VSYNC1 = VFP + VSYNC.

- **Vertical Offset (REG_VOFFSET):**

  Vertical offset defines total number of non-visible lines. REG_VOFFSET = VFP + VSYNC + VBP.

- **Vertical Active Display Area (REG_VSIZE):**

  The Vertical Active Display Area represents the number of visible lines transmitted per frame. It defines the vertical resolution of the display panel and corresponds to the portion of the frame where actual image data is presented. REG_VSIZE = VAD.

- **Vertical Cycle (REG_VCYCLE):**

  Vertical cycle defines the total number of lines (visible and non-visible) per frame. REG_VCYCLE = VSYNC + VBP + VAD + VFP.

4.4 Scanout Mode Setting

The BT820B supports up to four RGB pixel streams which are routed to the LVDS transmit channels. This routing is controlled via the REG_SO_MODE register. Table 8 summarizes the available scanout configurations.

SO_MODE [2:0]	Description
000	1-pixel per clock for single LVDS channel mode
001	2-pixel per clock for single LVDS channel mode
010	2-pixel per clock for dual LVDS channel mode
011	4-pixel per clock for dual LVDS channel mode

Table 8 - SO_Mode Configuration

Note:

- When REG_SO_MODE is set to 001 or 010, the following registers must contain even values: REG_HCYCLE, REG_HOFFSET, REG_HSYNC0, and REG_HSYNC1.

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- When REG_SO_MODE is 011, all of the above registers must be set to a multiple of 4 to maintain pixel alignment and avoid scan artifacts.

4.5 Matching Video Standard and Bitmap Format

To ensure proper image output, designers must configure the BT820B's video interface to match the specific requirements of the target LCD panel, including **LVDS signal format** and **bitmap data format**.

4.5.1 Video Standard Configuration

The BT820B supports up to two LVDS output channels, each comprising four data lanes. These are capable of transmitting video in either **18-bit** or **24-bit RGB formats**. The pixel format and lane assignment are controlled using the register:

- LVDS_REG.LVDS_CTRL_CH*.CH*_LVDS_MODE[1:0]

Configuration options are detailed in Table 9 - LVDS Output Mode Assignment for VESA and JEIDA Formats, while examples of 24-bit data mapping for both JEIDA and VESA formats are illustrated in Figure 19.

LVDS_MODE [1:0]	Description
11	VESA/Format 2 Mapping for 18-bit, Single Pixel per Clock Input
10 (default)	VESA/Format 2 Mapping for 24-bit, Single Pixel per Clock Input
01	JEIDA/Format 1 Mapping for 24-bit, Single Pixel per Clock Input A
00	JEIDA/Format 1 Mapping for 18-bit, Single Pixel per Clock Input

Table 9 - LVDS Output Mode Assignment for VESA and JEIDA Formats

Figure 19 - 24-bit JEIDA/VESA Format

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4.5.2 Bitmap Format Selection

The BT820B LVDS transmitter supports the following bitmap formats as the source of framebuffer:

- **RGB6** – 6 bits per color channel (18 bits per pixel)
- **RGB8** – 8 bits per color channel (24 bits per pixel)
- **YCbCr** – 8 bits per pixel

To configure the bitmap format, use the register:

- REG_SO_FORMAT

Ensure that the selected bitmap format is compatible with the target LCD panel's specifications. Incorrect bitmap configuration may result in colour distortion or display errors.

Designer may refer to BT820B datasheet and BT820B Programming Guide for further detail.

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5 Configuration Example

This section presents an example configuration of timing parameters, clock settings, and mode selections for a high-resolution 1920 × 1200 LCD panel operating in dual-channel, 24-bit, VESA format. Refer to Table 10 and Figure 20 for the required LCD timing specifications and data input format. Note that the LCD horizontal timings are specified based on one LVDS channel (odd or even channel).

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK Frequency	Fdclk	74.5	77.56	85	MHz
Horizontal display area	Thd		960		DCLK
HSYNC period time	Th	989	1040	1248	DCLK
Horizontal Blank	THB	29	80	288	DCLK
HSYNC pulse width	Thp	2	10	255	DCLK
HSYNC back porch	thbp	3	6	255	DCLK
HSYNC Front porch	thfp	24	64	260	DCLK
Vertical display area	Tvd		1200		H
VSYNC period time	Tv	1243	1243	1560	H
Vertical Blank	TVB	43	43	360	H
VSYNC Pluse width	Tvp	4	4	20	H
VSYNC back porch	Tvbp	20	20	255	H
VSYNC front porch	Tvfp	19	19	260	H
Frequency	fV	-	60	-	Hz

Table 10 - LCD Timing Requirement

LVDS data mapping

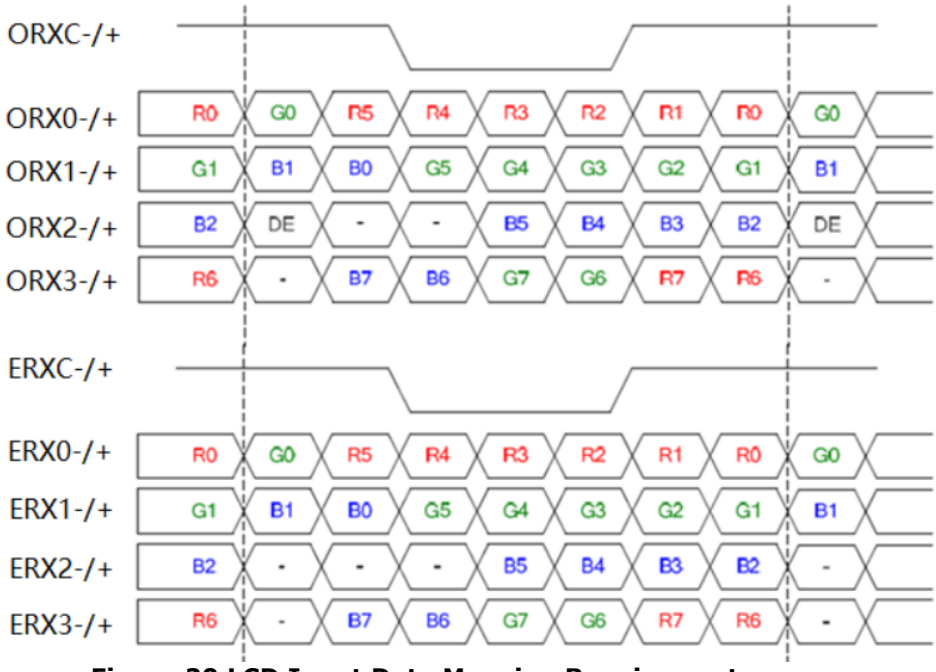

Figure 20 LCD Input Data Mapping Requirement

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Adjusting PCLK:

To meet the specified PCLK operating frequency range of 74.5 MHz to 85 MHz, refer to Table 7 - PCLK and LVDSTX Clock Configuration. In this case, it is necessary to modify the default value of **SYSPLL.NS** to 13 and set **TXCLKDIV** to 2 (corresponding to a division factor of 3), which results in a generated PCLK frequency of approximately 83.2 MHz

Hsync Pulse:

The Hsync pulse width can be configured within a range of 2 to 255 clock cycles, with a typical setting of 10 PCLK cycles. Though typical value calls for 10, it is recommended to use the typical value of 12*Note.

Note: REG_SO_MODE being set to 3 requires REG_HCYCLE, REG_HOFFSET, REG_HSYNC0 and REG_HSYNC1 to be set to multiples of 4.

Horizontal Back Porch:

The horizontal back porch can be set within a range of 3 to 255 clock cycles with typical value of 6 PCLK cycles, set value to 8 (for multiple of 4).

Horizontal Front Porch:

The horizontal front porch supports a range of 24 to 260 clock cycles. A typical setting of 64 PCLK cycles is recommended.

Vsync Pulse:

The Vsync pulse width can be configured between 4 and 20 lines. The panel calls for setting typical value to the minimum value of 4 lines.

Vertical Back Porch:

The vertical back porch allows a range of 20 to 255 lines The panel calls for setting typical value to the minimum value of 20 lines.

Vertical Front Porch:

The vertical front porch supports a range of 19 to 260 lines. The panel calls for setting typical value to the minimum value of 19 lines.

Video Standard Configuration:

Referencing the data mapping shown in Figure 20, configure the pixel format and lane assignment by setting the register REG_LVDSTX_CTRL_CH*.CH*_LVDS_MODE [1:0] to 0x10 (default). This setting ensures compliance with the VESA standard and enables 24-bit RGB color output.

Scanout Mode:

According to the data mapping illustrated in Figure 20, configure the data output format by setting the REG_SO_MODE register to 0x11, corresponding to the "4-pixel per clock" mode for dual LVDS channel operation.

Bitmap Format Selection:

Set the bitmap format to RGB8 (8 bits per color channel) to enable 24-bit color output. Using RGB6 will reduce color depth and result in loss of color detail.

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6 Contact Information

Refer to https://brtchip.com/contact-us/ for contact information.

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Appendix A – References

Document References

BT820B datasheet

BT820B Programming Guide

TPS61500 datasheet

Acronyms and Abbreviations

Terms	Description
CTP	Capacitive Touch Panel
DC	Direct Current
DCLK	Data Clock
DSI	Display Serial Interface
eDP	Embedded Display Port
EVE	Embedded Video Engine
FB	Feedback
FPC	Flexible Printed Circuit
GPIO	General Purpose Input Output
HAD	Horizontal Active Display Area
HBP	Horizontal Back Porch
HDMI	High-Definition Multimedia Interface
HFP	Horizontal Front Porch
HOFFSET	Horizontal Offset
HSYNC	Horizontal Synchronization
I2C	Inter-Integrated Circuit
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface

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OVP	Over Voltage Protection
PCLK	Pixel Clock
PWM	Pulse Width Modulation
SO	Scan Out
SPI	Serial Peripheral Interface
SVGA	Super Video Graphics Array
TFT	Thin-Film Transistor
TX	Transmit
VAD	Vertical Active Display Area
VBP	Vertical Back Porch
VC	Video Core
VFP	Vertical Front Porch
VSYNC	Vertical Synchronization
WSVGA	Wide Super Video Graphics Array
WXGA	Wide Extended Graphics Array

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Appendix B – Revision History

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