BT820 Framebuffer based Embedded Video Engine

Datasheet

The BT820 is the 5th Generation Embedded Video Engine (EVE), an easy-to-use family of graphics controller targeted at embedded applications to generate advanced high-quality Human Machine Interfaces (HMIs). It has the following features:

- Graphics, video input, audio output, and touch control interface
- Unified memory model
- 24-bit RGB framebuffer up to 2048 x 2048 pixels
- Render engine to accelerate image processing tasks
- Render-to-bitmap capability
- Hardware INFLATE engine
- Hardware PNG decompression engine
- Supports 24-bit RGB and 32-bit RGBA
- Supports full-speed paletted bitmaps, and 32-bit RGBA palettes
- Supports playback of motion-JPEG encoded AVI videos
- Supports YCbCr frame buffer format
- Real-time processing for input video stream
- Supports 2 channels, each with 4 data lanes, LVDS transmit interface up to 1920x1200 pixel resolution
- Supports 2 channels, each with 4 data lanes, LVDS receive interface up to 1920x1200 pixel resolution
- Supports external DDR3 / DDR3L / LPDDR2 DRAM up to 4Gbit to speed up video processing
- Supports QSPI host interface in Single, Dual, or Quad mode up to 60MHz
- Supports QSPI NOR / NAND flash memory devices
- Supports SD Card Interface
- Supports an I2C master interface to external touch screen controller device.
- Supports auto discovery feature to discover attached touch controller
- Hardware touch engine to recognize touch tags and track touch movements with up to 5 touch point detection.
- Supports stereo audio channel outputs
- Supports I2S output interface
- Built-in sound synthesizer
- Integrated 32-bit watchdog timer
- Integrated 38.4MHz crystal oscillator with PLL providing a programmable system clock up to 72MHz
- Supports various low power modes
- Supports multiple I/O voltage of 1.8V, 2.5V or 3.3V
- Internal voltage regulator supplies 1.0V to the digital core
- Built-in Power-on-reset circuit
- -40°C to 85°C extended operating temperature range
- Available in a compact Pb-free, 329 Ball package, RoHS compliant

1 Typical Applications

- Point of Sales Machines
- Multi-function Printers
- Instrumentation
- Home Security Systems
- Graphic touch pad – remote, dial pad
- Tele / Video Conference Systems
- Phones and Switchboards
- Medical Appliances
- Blood Pressure displays
- Heart monitors
- Glucose level displays
- Automotive
- Digital Photo Frame
- Breathalyzers
- Gas chromatographs
- Power meter
- Home appliance devices
- Set-top box
- Thermostats
- Sprinkler system displays
- GPS / Satnav
- Vending Machine Control Panels
- Elevator Controls
- Interactive Photo Booth
- Smart Door Bell System
- ……and many more

1.1 Part Numbers

Part Number	Description	Package
BT820B	EVE5, 5th Generation Embedded Video Engine with DDR DRAM frame-buffer and dual-channel LVDS inputs and outputs	329 Ball LFBGA, 17x17x1.5mm

Table 1 - EVE5 Embedded Video Engine Part Numbers

2 Block Diagram

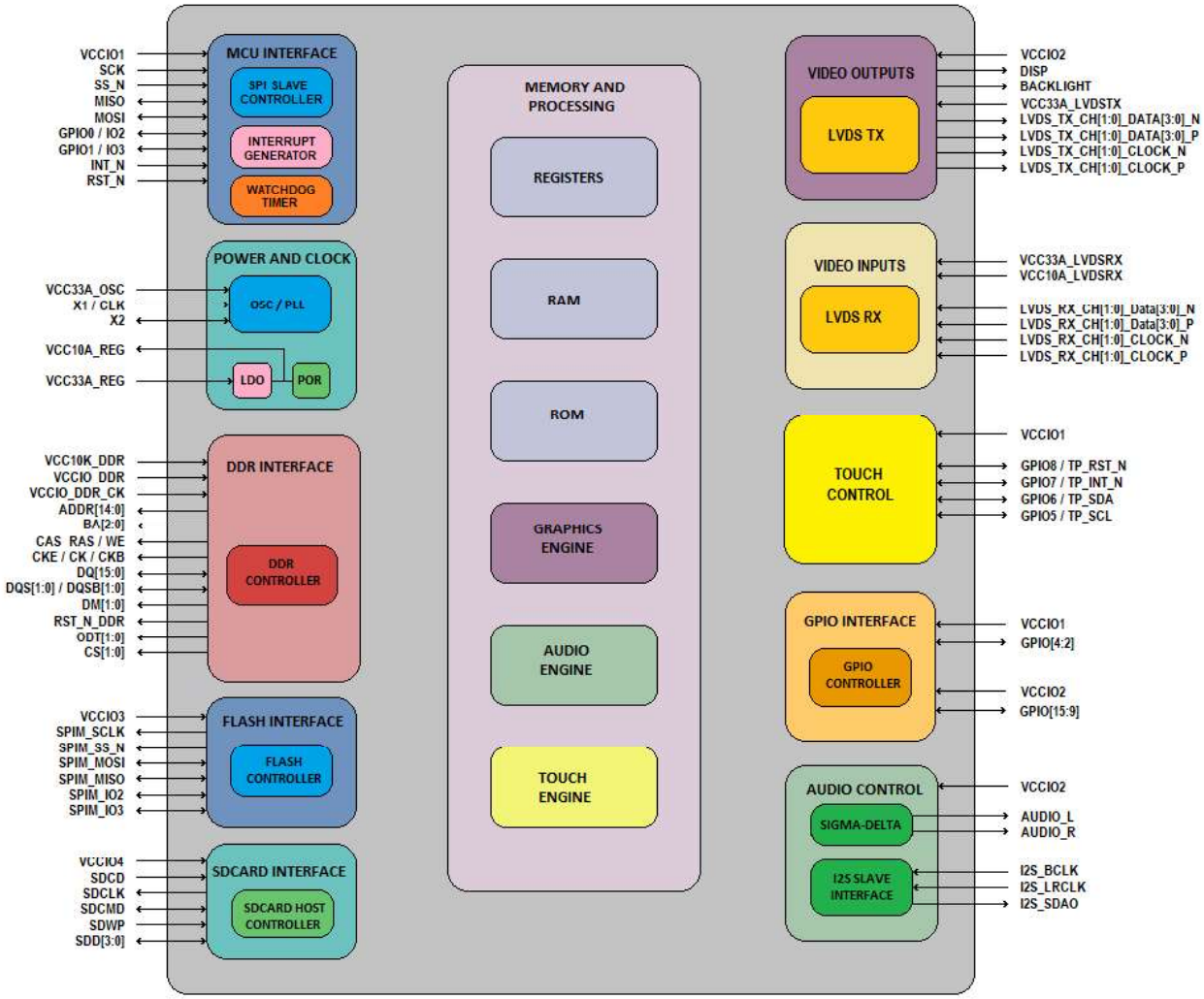


Figure 1 - BT820 Block Diagram

Please refer to Section 4 for descriptions of each function.

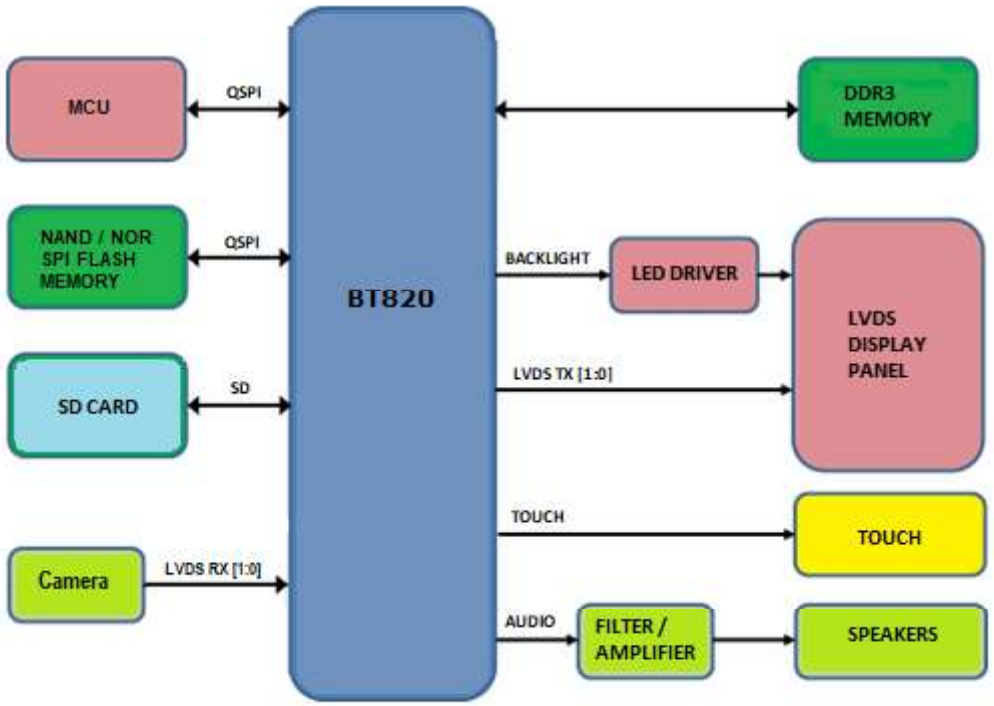


Figure 2 - BT820 System Design Diagram

BT820 with EVE (Embedded Video Engine) technology simplifies the system architecture for advanced human machine interfaces (HMIs) by providing support for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

Table of Contents

3 Device Pin Out and Signal Description

3.1 BT820B Package Pin Out

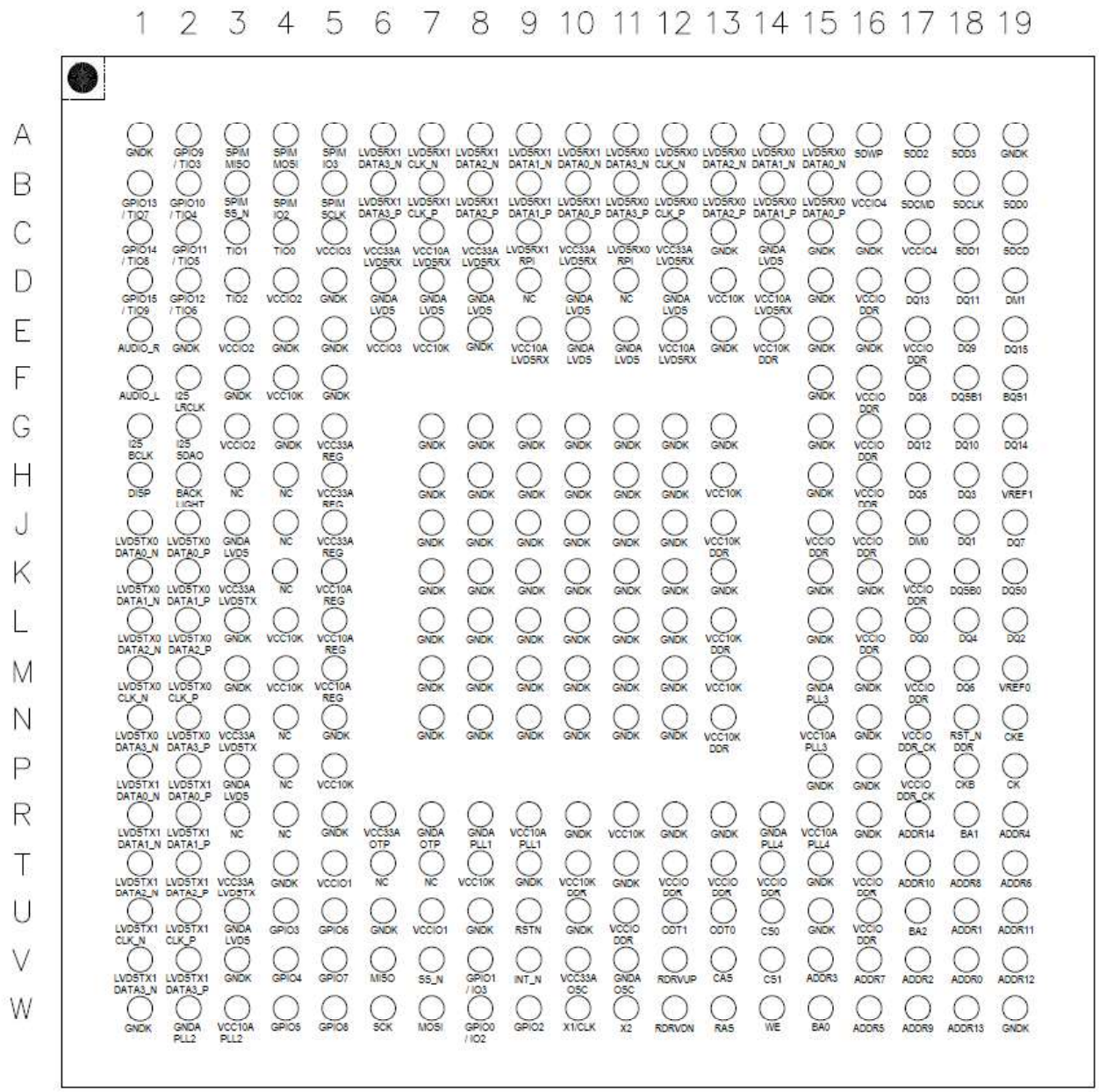


Figure 3 - Pin Configuration BT820B 329 BALLS LFBGA (Transparent Top View)

3.2 Pin Description

Ball Number	Ball Name	Type	Description
MCU Interface			
W6	SCK	I	SPI clock input
V7	SS_N	I	SPI slave select input
V6	MISO	I/O	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
W7	MOSI	I/O	SPI Single mode: SPI MOSI input SPI Dual/Quad mode: SPI data line 0
W8	GPIO0/IO2	I/O	SPI Single mode: General purpose IO 0 SPI Quad mode: SPI data line 2
V8	GPIO1/IO3	I/O	SPI Single mode: General purpose IO 1 SPI Quad mode: SPI data line 3
V9	INT_N	OD/O	Interrupt to host, open drain output (default) or push-pull output, active low
U9	RST_N	I	Global reset pin. Connect to MCU GPIO for hardware reset function, or pull up to VCCIO1 through 47 KΩ resistor and 1μF to ground
Flash Interface			
B5	SPIM_SCLK	O	SPI flash clock output line
B3	SPIM_SS_N	O	SPI flash chip-select output line
A3	SPIM_MISO	I/O	SPI flash MISO line
A4	SPIM_MOSI	I/O	SPI flash MOSI line
B4	SPIM_IO2	I/O	SPI flash IO2 line
A5	SPIM_IO3	I/O	SPI flash IO3 line
SD Card Interface			
C19	SDCD	I	SD Card Detect
B18	SDCLK	O	SD Card serial clock output
B17	SDCMD	I/O	SD Card Command signal
A16	SDWP	I	SD Card Write protection
B19	SDD0	I/O	SD Card Data bus line 0
C18	SDD1	I/O	SD Card Data bus line 1
A17	SDD2	I/O	SD Card data bus line 2
A18	SDD3	I/O	SD Card Data bus line 3
DDR Interface			
P19	CK	O	DDR DRAM clock differential P signal
P18	CKB	O	DDR DRAM clock differential N signal
L17	DQ0	I/O	DDR DRAM data bus bit 0
J18	DQ1	I/O	DDR DRAM data bus bit 1
L19	DQ2	I/O	DDR DRAM data bus bit 2
H18	DQ3	I/O	DDR DRAM data bus bit 3
L18	DQ4	I/O	DDR DRAM data bus bit 4
H17	DQ5	I/O	DDR DRAM data bus bit 5

Ball Number	Ball Name	Type	Description
M18	DQ6	I/O	DDR DRAM data bus bit 6
J19	DQ7	I/O	DDR DRAM data bus bit 7
F17	DQ8	I/O	DDR DRAM data bus bit 8
E18	DQ9	I/O	DDR DRAM data bus bit 9
G18	DQ10	I/O	DDR DRAM data bus bit 10
D18	DQ11	I/O	DDR DRAM data bus bit 11
G17	DQ12	I/O	DDR DRAM data bus bit 12
D17	DQ13	I/O	DDR DRAM data bus bit 13
G19	DQ14	I/O	DDR DRAM data bus bit 14
E19	DQ15	I/O	DDR DRAM data bus bit 15
K19	DQS0	I/O	DDR DRAM dqs for lower data byte
K18	DQSB0	I/O	DDR DRAM dqs# (diff mode) for lower data byte
F19	DQS1	I/O	DDR DRAM dqs for upper data byte
F18	DQSB1	I/O	DDR DRAM dqs# (diff mode) for upper data byte
J17	DM0	O	DDR DRAM data mask for lower data byte
D19	DM1	O	DDR DRAM data mask for lower data byte
V18	ADDR0	O	DDR DRAM address bit 0
U18	ADDR1	O	DDR DRAM address bit 1
V17	ADDR2	O	DDR DRAM address bit 2
V15	ADDR3	O	DDR DRAM address bit 3
R19	ADDR4	O	DDR DRAM address bit 4
W16	ADDR5	O	DDR DRAM address bit 5
T19	ADDR6	O	DDR DRAM address bit 6
V16	ADDR7	O	DDR DRAM address bit 7
T18	ADDR8	O	DDR DRAM address bit 8
W17	ADDR9	O	DDR DRAM address bit 9
T17	ADDR10	O	DDR DRAM address bit 10
U19	ADDR11	O	DDR DRAM address bit 11
V19	ADDR12	O	DDR DRAM address bit 12
W18	ADDR13	O	DDR DRAM address bit 13
R17	ADDR14	O	DDR DRAM address bit 14
W15	BA0	O	DDR DRAM bank address bit 0
R18	BA1	O	DDR DRAM bank address bit 1
U17	BA2	O	DDR DRAM bank address bit 2
W13	RAS	O	DDR DRAM command input
V13	CAS	O	DDR DRAM command input
W14	WE	O	DDR DRAM command input
N19	CKE	O	DDR DRAM clock enable

Ball Number	Ball Name	Type	Description
U14	CS0	O	DDR DRAM chip select bit 0
V14	CS1	O	DDR DRAM chip select bit 1
U13	ODT0	O	DDR DRAM ODT resistor control bit 0
U12	ODT1	O	DDR DRAM ODT resistor control bit 1
N18	RST_N_DDR	O	DDR DRAM reset for DDR3 mode
M19	VREF0	AI/O	DDR reference voltage for lower data byte receivers. Connect a voltage that is half the voltage of VCCIO_DDR.
H19	VREF1	AI/O	DDR reference voltage for lower data byte receivers. Connect a voltage that is half the voltage of VCCIO_DDR.
W12	RDRVDN	AI/O	DDR pad to precise external resistor for pull-down driver. Tie to DDR I/O power via 240Ω external resistor with 1% tolerance
V12	RDRVUP	AI/O	DDR pad to precise external resistor for pull-up driver. Tie to GND via 240Ω external resistor with 1% tolerance
Video Output			
H1	DISP	O	LCD display general purpose control (e.g., enable/reset) signal
H2	BACKLIGHT	O	LED backlight brightness PWM control signal
M1	LVDSTX0_CLK_N	O	LVDS TX channel 0 clock differential N signal
M2	LVDSTX0_CLK_P	O	LVDS TX channel 0 clock differential P signal
U1	LVDSTX1_CLK_N	O	LVDS TX channel 1 clock differential N signal
U2	LVDSTX1_CLK_P	O	LVDS TX channel 1 clock differential P signal
J1	LVDSTX0_DATA0_N	O	LVDS TX channel 0 data bit 0 differential N signal
J2	LVDSTX0_DATA0_P	O	LVDS TX channel 0 data bit 0 differential P signal
K1	LVDSTX0_DATA1_N	O	LVDS TX channel 0 data bit 1 differential N signal
K2	LVDSTX0_DATA1_P	O	LVDS TX channel 0 data bit 1 differential P signal
L1	LVDSTX0_DATA2_N	O	LVDS TX channel 0 data bit 2 differential N signal
L2	LVDSTX0_DATA2_P	O	LVDS TX channel 0 data bit 2 differential P signal
N1	LVDSTX0_DATA3_N	O	LVDS TX channel 0 data bit 3 differential N signal
N2	LVDSTX0_DATA3_P	O	LVDS TX channel 0 data bit 3 differential P signal
P1	LVDSTX1_DATA0_N	O	LVDS TX channel 1 data bit 0 differential N signal
P2	LVDSTX1_DATA0_P	O	LVDS TX channel 1 data bit 0 differential P signal
R1	LVDSTX1_DATA1_N	O	LVDS TX channel 1 data bit 1 differential N signal
R2	LVDSTX1_DATA1_P	O	LVDS TX channel 1 data bit 1 differential P signal
T1	LVDSTX1_DATA2_N	O	LVDS TX channel 1 data bit 2 differential N signal
T2	LVDSTX1_DATA2_P	O	LVDS TX channel 1 data bit 2 differential P signal
V1	LVDSTX1_DATA3_N	O	LVDS TX channel 1 data bit 3 differential N signal
V2	LVDSTX1_DATA3_P	O	LVDS TX channel 1 data bit 3 differential P signal
Video Input			
A12	LVDSRX0_CLK_N	I	LVDS RX channel 0 clock differential N signal

Ball Number	Ball Name	Type	Description
B12	LVDSRX0_CLK_P	I	LVDS RX channel 0 clock differential P signal
A7	LVDSRX1_CLK_N	I	LVDS RX channel 1 clock differential N signal
B7	LVDSRX1_CLK_P	I	LVDS RX channel 1 clock differential P signal
A15	LVDSRX0_DATA0_N	I	LVDS RX channel 0 data bit 0 differential N signal
B15	LVDSRX0_DATA0_P	I	LVDS RX channel 0 data bit 0 differential P signal
A14	LVDSRX0_DATA1_N	I	LVDS RX channel 0 data bit 1 differential N signal
B14	LVDSRX0_DATA1_P	I	LVDS RX channel 0 data bit 1 differential P signal
A13	LVDSRX0_DATA2_N	I	LVDS RX channel 0 data bit 2 differential N signal
B13	LVDSRX0_DATA2_P	I	LVDS RX channel 0 data bit 2 differential P signal
A11	LVDSRX0_DATA3_N	I	LVDS RX channel 0 data bit 3 differential N signal
B11	LVDSRX0_DATA3_P	I	LVDS RX channel 0 data bit 3 differential P signal
A10	LVDSRX1_DATA0_N	I	LVDS RX channel 1 data bit 0 differential N signal
B10	LVDSRX1_DATA0_P	I	LVDS RX channel 1 data bit 0 differential P signal
A9	LVDSRX1_DATA1_N	I	LVDS RX channel 1 data bit 1 differential N signal
B9	LVDSRX1_DATA1_P	I	LVDS RX channel 1 data bit 1 differential P signal
A8	LVDSRX1_DATA2_N	I	LVDS RX channel 1 data bit 2 differential N signal
B8	LVDSRX1_DATA2_P	I	LVDS RX channel 1 data bit 2 differential P signal
A6	LVDSRX1_DATA3_N	I	LVDS RX channel 1 data bit 3 differential N signal
B6	LVDSRX1_DATA3_P	I	LVDS RX channel 1 data bit 3 differential P signal
C11	LVDSRX0_RPI	I	LVDS RX channel 0 bias. Connects 3.5 KΩ external resistor to GND.
C9	LVDSRX1_RPI	I	LVDS RX channel 1 bias. Connects 3.5 KΩ external resistor to GND.
Touch Control			
U4	GPIO3	I/O	General purpose IO 3
V4	GPIO4	I/O	General purpose IO 4
W4	GPIO5 / TP_SCL	I/O	General purpose IO 5 / I2S_SCL for Touch Control
U5	GPIO6 / TP_SDA	I/O	General purpose IO 6 / I2C_SDA for Touch Control
V5	GPIO7 / TP_INT_N	I/O	General purpose IO 7 / INT_N for Touch Control
W5	GPIO8 / TP_RST_N	I/O	General purpose IO 8 / RST_N for Touch Control
Audio Control			
F1	AUDIO_L	O	Audio Delta-Sigma left output
E1	AUDIO_R	O	Audio Delta-Sigma right output
G1	I2S_BCLK	I	I2S bit clock
F2	I2S_LRCLK	I	I2S left/right clock
G2	I2S_SDAO	O	I2S serial data output
GPIO Interface			
W9	GPIO2	I/O	General purpose IO 2
A2	GPIO9 / TIO3	I/O	General purpose IO 9
B2	GPIO10 / TIO4	I/O	General purpose IO 10

Ball Number	Ball Name	Type	Description
C2	GPIO11 / TIO5	I/O	General purpose IO 11
D2	GPIO12 / TIO6	I/O	General purpose IO 12
B1	GPIO13 / TIO7	I/O	General purpose IO 13
C1	GPIO14 / TIO8	I/O	General purpose IO 14
D1	GPIO15 / TIO9	I/O	General purpose IO 15
Clock Interface			
W10	X1/CLK	AI	Crystal oscillator or clock input. 3.3V peak input allowed
W11	X2	AI/O	Crystal oscillator output
Power			
G5, H5, J5	VCC33A_REG	P	3.3V Analog supply for Linear Regulator. A 47uF capacitor must be connected between VCC33A_REG and GND
K5, L5, M5	VCC10A_REG	P	1.0V output voltage from Linear Regulator. Connect a 3.3uF decoupling capacitor
D13, E7, F4, H13, L4 M4, M13, T8 R11, P5	VCC10K	P	1.0V digital core power supply
T5, U7	VCCIO1	P	I/O power supply for host interface pins. Support 1.8V, 2.5V or 3.3V
D4, E3, G3	VCCIO2	P	3.3V I/O power supply for Display, I2S and Audio
C5, E6	VCCIO3	P	I/O power supply for SPIM interface pins. Support 1.8V, 2.5V or 3.3V
B16, C17	VCCIO4	P	I/O power supply for SD interface pins. Support 1.8V, 2.5V or 3.3V
K3, N3, T3	VCC33A_LVDSTX	P	3.3V Analog supply for LVDS TX
C6, C8, C10, C12	VCC33A_LVDSRX	P	3.3V Analog supply for LVDS RX
C7, D14, E9, E12	VCC10A_LVDSRX	P	1.0V Analog supply for LVDS RX
E14, J13, L13, T10, N13	VCC10K_DDR	P	1.0V digital power supply for DDR PHY
D16, E17, F16, G16, H16, J15, J16, K17, L16, M17, T12, T13, T14, T16, U11, U16	VCCIO_DDR	P	Digital I/O power supply for DDR PHY
N17, P17	VCCIO_DDR_CK	P	Digital I/O power supply for DDR CK/CKB and CKE
R6	VCC33A_OTP	P	3.3V I/O power supply for OTP
V10	VCC33A_OSC	P	3.3V Analog power supply for OSC pad
R9	VCC10A_PLL1	P	1.0V Analog power supply for PLL1
W3	VCC10A_PLL2	P	1.0V Analog power supply for PLL2
N15	VCC10A_PLL3	P	1.0V Analog power supply for PLL3
R15	VCC10A_PLL4	P	1.0V Analog power supply for PLL4
Ground			
A1, A19, C13, C15, C16, D5, D15, E2, E4, E5, E8, E13,	GNDK	P	Digital Ground

Ball Number	Ball Name	Type	Description
E15, E16, F3, F5, F15, G4, G7, G8, G9, G10, G11 G12, G13, G15 H7, H8, H9, H10, H11, H12, H15, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, K13, K15, K16, L3, L7, L8, L9, L10, L11, L12, L15, M3, M7, M8, M9, M10, M11, M12, M16, N5, N7, N8, N9, N10, N11, N12, N16, P15, P16, R5, R10, R12, R13, R16, T4, T9, T11, T15, U6, U8, U10, U15, V3, W1, W19			
C14, D6, D7, D8, D10, D12, E10, E11, J3, P3, U3	GNDA_LVDS	P	LVDS Analog Ground
R7	GNDA_OTP	P	Analog ground for OTP
V11	GNDA_OSC	P	Analog ground for OSC
R8	GNDA_PLL1	P	Analog ground for PLL1
W2	GNDA_PLL2	P	Analog ground for PLL2
M15	GNDA_PLL3	P	Analog ground for PLL3
R14	GNDA_PLL4	P	Analog ground for PLL4
Test Pins			
C4	TIO0	I/O	Test pin bit 0. To be left unconnected
C3	TIO1	I/O	Test pin bit 1. To be left unconnected
D3	TIO2	I/O	Test pin bit 2. To be left unconnected
No Connections			
D9, D11, H3, H4, J4, N4, P4, R3, R4, T6, T7, K4	NC	NC	No Connections

Table 2 - BT820B Pin Description

Note:
P : Power or ground
I : Input
O : Output
OD : Open drain output
I/O : Bi-direction Input and Output
AI/O : Analog Input and Output
NC : No connection and must be left open/floating

4 Functional Description

The BT820 is a single chip, embedded video controller with the following functional blocks:

- Graphics Engine
- LVDS Transmit Interface
- LVDS Receive Interface
- DDR DRAM Interface
- Quad SPI Host Interface
- Quad SPI Flash Interface
- SD Card Host Controller
- Touch Engine and Interface
- Audio Engine
- Audio Outputs / Interface
- Watchdog Timer
- System Clock
- General Purpose IO (GPIO) Pins
- Power Management

The functions for each block are briefly described in the following subsections.

4.1 Graphics Engine

4.1.1 Introduction

The graphics engine executes the display list once for every frame. The BT820 includes a 16Kbytes double-buffered memory within its graphics engine, dedicated to storing display list commands. The display list can contain between 1 and 4096 commands, each of which sets the graphics state, performs a drawing action, or controls the execution flow within the list. The graphics engine then executes the primitive objects in the display list and constructs the display frame buffer.

Main features of the graphics engine are:

- The primitive objects supported by the graphics processor are lines, points, rectangles, bitmaps (comprehensive set of formats), text display, plotting bar graph, edge strips, line strips, etc
- Operations such as stencil test, alpha blending and masking are useful for creating a rich set of effects such as shadow, transitions, reveals, fades, and wipes
- Anti-aliasing of the primitive objects (except bitmaps) gives a smoothing effect to the viewer
- Bitmap transformations enable operations such as translate, scale, and rotate
- Display pixels are plotted with 1/16th pixel resolution
- Four levels of graphics states
- Tag buffer for touch detection

The graphics engine also supports customized built-in widgets and functionalities. The graphics engine reads and executes the commands from the MCU. This is done by accessing the command FIFO. Refer to BRT AN086 BT82X Series Programming Guide for details to access the graphics engine.

The graphics engine used in BT820 has many improvements over the one in BT81x series:–

- Unified memory model, supporting an address space up to 512MBytes
- 24-bit RGB framebuffer up to 2048 x 2048 pixels
- Render-to-bitmap capability
- Hardware INFLATE engine
- Hardware PNG decode engine
- YCbCr format support
- 24-bit RGB and 32-bit RGBA bitmap support
- Full-speed palette bitmaps, and 32-bit RGBA palettes

Other features supported are:

- Drawing of widget such as ARC, buttons, clock, keys, gauges, text displays, progress bars, sliders, toggle switches, dials, gradients, etc

- JPEG and motion-JPEG decode
- Snapshot feature to capture the current graphics display
- ASTC decode

4.1.2 Hardware INFLATE Engine

The BT820 features a hardware INFLATE Engine that decompresses application-specific assets that may be supplied in the command buffer, the media fifo, or from the external flash, and transfers the results to either the graphics engine or DDR memory. The hardware INFLATE engine greatly accelerates the decompression process.

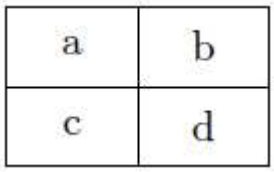
These assets can be compressed using the Asset Compressor feature in the EVE Asset Builder.

4.1.3 Hardware PNG decode Engine

The hardware PNG decode engine featured in the BT820 is designed to efficiently decode the Portable Network Graphics (PNG) images.

4.1.4 YCbCr Format

BT820 supports YCbCr encoding and YCbCr decoding. The YCbCr format is a lossy pixel format using 1 byte per pixel. The pixels are encoded in 2 x 2 blocks, each taking 32 bits of memory.



The YCbCr is particularly suited to JPEG output, but is also effective as a framebuffer format with very little loss in quality. There are three encoding variants, depending on the distribution of Y pixels in the quad. The 5-bit chroma encoding is most frequently used, with 6- and 8-bit chroma used for quad with similar Y values. This improves color fidelity in image regions with little luminance detail.

4.1.5 Render Engine

The BT820 render engine excels in memory-to-memory operations, leveraging local memory access for bulk memory and image processing tasks. This local optimization translates to significant speed advantage in data handling and rendering tasks, avoiding the SPI bottleneck inherent in using the microcontroller.

The render engine supports a maximum bitmap size of 2048 x 2048 and a maximum bitmap linestride of 8192 bytes.

4.1.6 ASTC

ASTC stands for **A**daptive **S**calable **T**exture **C**ompression, an open standard developed by ARM for use in mobile GPUs.

ASTC is a block-based lossy compression format. The compressed image is divided into a number of blocks of uniform size, which makes it possible to quickly determine which block a given texel (unit of a texture map) resides in. Each block has a fixed memory footprint of 128 bits, but these bits can represent varying numbers of texels (the block footprint).

Block footprint sizes are not confined to power-of-two, and are also not confined to be square. For 2D formats, the block dimensions range from 4 to 12 texels.

Using ASTC for the large ROM fonts can save considerable space. Encoding the four largest fonts in ASTC 8x8 formats gives no noticable loss in quality and reduces the ROM size from 1 Mbytes to about 640 Kbytes.

4.1.7 ROM and RAM Fonts

The BT820 has built-in ROM character bitmaps as font metrics. The graphics engine can use these metrics when drawing text fonts. There are a total of 19 ROM fonts, numbered with font handle 16-34. Font 31-34 are large ROM fonts encoded in ASTC 8x8 format. The user can define and load customized font metrics into the DDR memory or external flash, making it possible to support a full range of unicode characters with UTF-8 coding points.

The BT820 recognizes two in-memory font structures. A legacy format handles fonts with code points 0x0 to 0x7F. An extended format can handle fonts with a full range of unicode code points.

4.1.7.1 Legacy Format

Each ROM font metric block has a 148 byte font table which defines the parameters of the font and the pointer of font image. The Legacy font metric block is listed in Table 3.

Address Offset	Size	Value
0	128	Width of each font character, in pixels
128	2	Font bitmap format, for example L1, L4 or L8
130	2	Font flag (see below)
132	4	Font line stride, in bytes
136	4	Font width, in pixels
140	4	Font height, in pixels
144	4	Pointer to font graphic data in memory

Table 3 – Legacy Format

4.1.7.2 Extended Format

The font for the Extended block is variable-sized, depending on the number of characters.

Refer to BRT AN086 BT82X Series Programming Guide for details on how to access the Extended format.

4.1.7.3 ROM fonts

The ROM fonts are loaded at startup into handles 16-34. These fonts can be loaded into arbitrary handles and the font handles can be reset to their startup defaults.

Each font contains 95 printable ASCII characters ranging from 0x20 to 0x7E, which correspond to their respective ASCII values.

Table 4 lists the ROM font handles.

handle	em-width	em-height	note
16	8	8	1-bit, monospace
17	8	8	1-bit, monospace (Extended ASCII characters)
18	8	16	1-bit, monospace
19	8	16	1-bit, monospace (Extended ASCII characters)
20	10	13	1-bit, proportional
21	13	17	1-bit, proportional
22	14	20	1-bit, proportional
23	17	22	1-bit, proportional
24	24	29	1-bit, proportional
25	30	38	1-bit, proportional
26	14	16	anti-aliased, proportional with kerning
27	15	18	anti-aliased, proportional with kerning
28	18	22	anti-aliased, proportional with kerning
29	22	27	anti-aliased, proportional with kerning
30	28	33	anti-aliased, proportional with kerning
31	38	46	anti-aliased, proportional with kerning
32	48	58	anti-aliased, proportional with kerning

33	62	74	anti-aliased, proportional with kerning
34	83	98	anti-aliased, proportional with kerning

Table 4 – ROM font handles

Note: The em-width and em-height are the size of uppercase "M" character in pixels.

A 1-bit monospace font is a type of font where each character is displayed using only two colours (black and white), and every character occupies the same horizontal space. In contrast, a 1-bit proportional font also uses two colours, but the characters have varying widths, taking up only as much horizontal space as needed, which enhances readability and aesthetic appeal.

Anti-aliased proportional fonts with kerning are a type of proportional font where the anti-aliasing technique smooths the edges of characters, reducing jagged edges on diagonal or curved lines by blending them with the background. Kerning adjusts the spacing between specific pairs of characters to ensure consistent and balanced spacing, making the text look more professional and easier to read.

4.1.7.4 Using Custom Font

The custom fonts are loaded into the DDR memory and the new fonts can be registered with handle 0-63 using internal commands. Refer to BRT AN086 BT82X Series Programming Guide for details on how to program the custom fonts.

4.2 Video Outputs

The BT820 support video streams up to 1920x1200 resolution at 60fps. The video output consists of the ExtSync and the LVDS transmit interface.

4.2.1 ExtSync

The function of the ExtSync is to bridge the graphics engine output to the LVDS transmit interface at different scanout frequencies. It achieves this by buffering the video streams and then transferring them to the LVDS transmit interface with the generated LVDSTX clock.

4.2.2 LVDS Transmit Interface

The BT820 implements 2 LVDS channels of 4 data lanes each to transmit 18 or 24-bit RGB signals. The BT820 supports a programmable PCLK, up to 83.2MHz. This allows the BT820 to support a wider range of display panels, up to 1920x1200 resolution at 60fps.

Four video modes are implemented:

- VESA / Format 2 Mapping for 18-bit RGB
- VESA / Format 2 Mapping for 24-bit RGB
- JEIDA / Format 1 Mapping for 18-bit RGB
- JEIDA / Format 1 Mapping for 24-bit RGB

Figure 4 shows the video formats for VESA / Format 2 Mappings for 24-bit RGB, Figure 5 shows the video formats for JEIDA / Format 1 Mappings for 24-bit RGB, Figure 6 shows the video formats for JEIDA / Format 1 Mapping for 18-bit RGB.

Figure 4 – VESA / Format 2 Mapping for 24-bit RGB

Figure 5 – JEIDA / Format 1 Mapping for 24-bit RGB

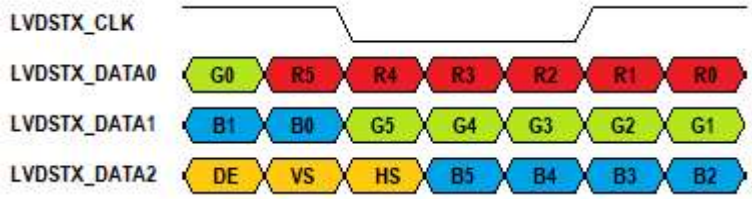


Figure 6 – JEIDA / Format 1 Mapping for 18-bit RGB

VESA / Format 2 Mapping for 24-bit RGB is implemented as the default for both LVDS channels

BT820 supports 2 LVDS transmit channels, LVDSTX0 and LVDSTX1. When using dual channels LVDS display, LVDSTX0 is the odd channel while LVDSTX1 is the even channel. When using single channel LVDS display, only LVDSTX0 is operational.

4.3 LVDS Receive Interface

The BT820 implements 2 LVDS channels of 4 data lanes to capture 18 or 24-bit RGB signals.

Three video modes are supported:

- VESA / Format 2 Mapping for 24-bit RGB
- JEIDA / Format 1 Mapping for 24-bit RGB
- JEIDA / Format 1 Mapping for 18-bit RGB

The BT820 can receive up to 1920x1200 resolution at 60fps

When capturing from dual LVDS channels, LVDSRX0 is the odd channel while LVDSRX1 is the even channel. When capturing from single LVDS channel, only LVDSRX0 is operational.

The maximum input clock for the LVDS receive channels are 144MHz at 72MHz system clock.

4.4 DDR DRAM Interface

The BT820 includes a DDR DRAM interface to allow the core to use an external DDR DRAM as a frame buffer. This allows the core to speed up video processing and allows support for higher resolution processing.

BT820 supports external DDR3, DDR3L, and LPDDR2 DRAM with data rates of 933MT/s, 1066MT/s and 1333MT/s for DDR3 and DDR3L, and 800MT/s and 933MT/s for LPDDR2, with data bit width of 16 bits only. It supports DRAM size of 8 Gbit, 4 Gbit, 2 Gbit, 1 Gbit and 512 Mbit. Support for 8 Gbit DRAM is limited to the use of 2 ranks of 4 Gbit DRAM.

By default, the BT820 supports 1Gbit DDR3, DDR3L with data rate of 1333MT/s

The BT820 includes a configuration parameter in the host command to set the DDR type, size, and speed grade to match the physical memory. For detailed instructions on setting the DDR type, size, and speed grade, refer to the BRT AN086 BT82X Series Programming Guide.

Table 5 lists the tested DDR memories that are tested at 1333MT/s

Brand	Model	Type	Description
Winbond	W631GU6NB-11	DDR3L	1Gbit (8M x 8 Banks x 16 Bit) DDR3L SDRAM
	W631GU6RB-11	DDR3L	1Gbit (8M x 8 Banks x 16 Bit) DDR3L SDRAM
	W634GU6RB-11	DDR3L	4Gbit (32M x 8 Banks x 16 Bit) DDR3L SDRAM
Micron	MT41K256M16TW-107	DDR3L	4Gbit (32M x 8 Banks x 16 Bit) DDR3L SDRAM
	MT41K128M16JT-107	DDR3L	2Gbit (16M x 8 Banks x 16 Bit) DDR3L SDRAM
	MT41K64M16TW-107	DDR3L	1Gbit (8M x 8 Banks x 16 Bit) DDR3L SDRAM

Table 5 – List of tested DDR Memories

4.5 Quad SPI Host Interface

The BT820 uses the Quad SPI (QSPI) Host Interface, operating in slave mode, to communicate with the host microcontroller and microprocessor, which serve as the master.

The QSPI Host Interface operates up to 60MHz and only supports SPI mode 0, where data is sampled on the rising edge of SCK. The QSPI Host Interface can be configured as SPI Single, Dual, or Quad channel modes. By default, the interface operates in Single channel mode with the MOSI as input from the master and MISO as output to the master. The interface can then be configured to Dual or Quad channel mode by programming the internal registers of the BT820. Refer to BRT AN086 BT82X Series Programming Guide for details on how to reconfigure the QSPI Host Interface to Dual or Quad channel modes. In Dual channel mode, MISO (MSB) and MOSI are used as data ports while in Quad channel mode, IO3 (MSB), IO2, MISO and MOSI are used as data ports. The SPI data ports are bi-directional in Dual and Quad channel modes.

Figure 7 illustrates a direct connnection to a MCU using Single SPI, Figure 8 illustrates a direct connection to a MCU using Dual SPI and Figure 9 illustrates a direct connection to a MCU using Quad SPI.

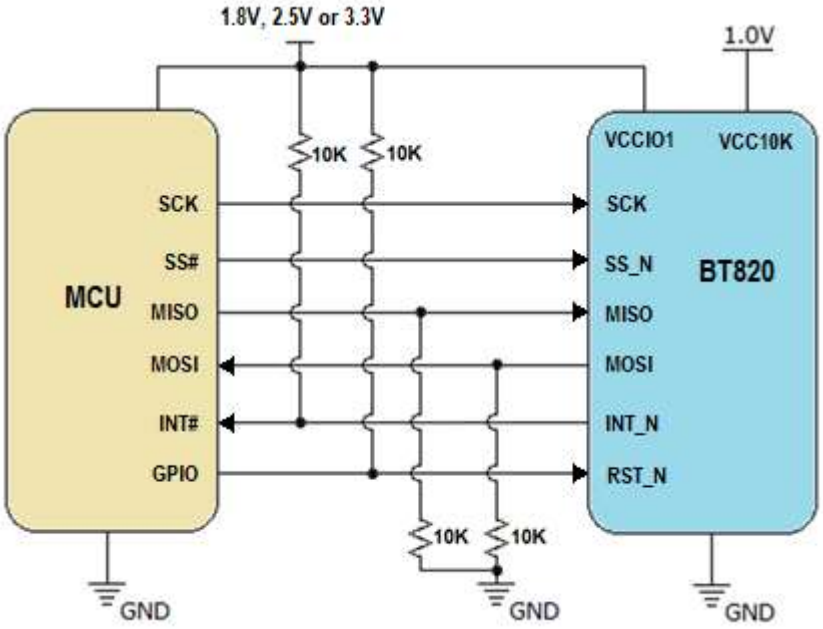


Figure 7 – QSPI Host Interface Using Single SPI Connection

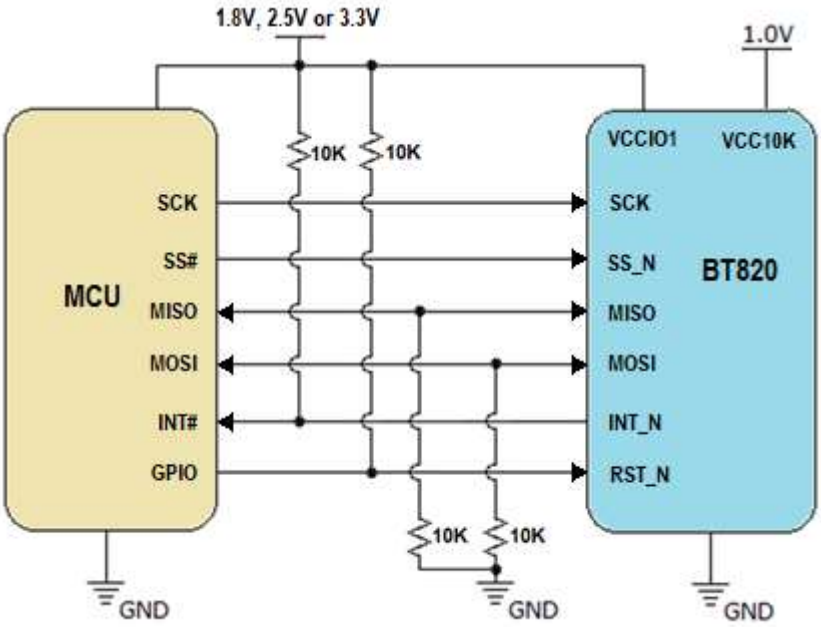


Figure 8 – QSPI Host Interface Using Dual SPI Connection

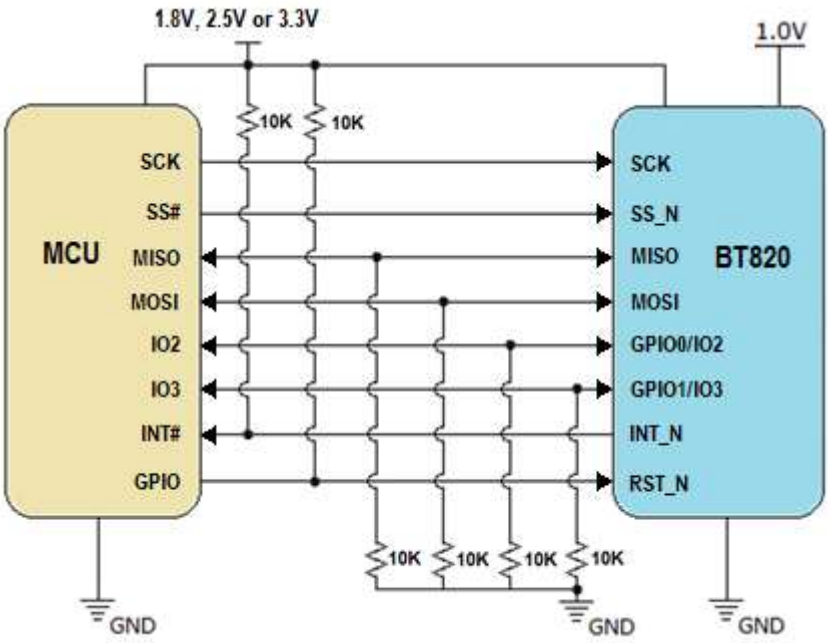


Figure 9 – QSPI Host Interface Using Quad SPI Connection

The QSPI Host Interface is powered by VCCIO1, which can accept power supply inputs of 1.8V, 2.5V or 3.3V. This allows the BT820 to match VCCIO1 with the MCU's I/O voltage.

4.5.1 QSPI Host Interface Protocol

In contrast to the QSPI host interface for the BT81x, which supports 22 bit addressing, the QSPI host interface for the BT820 supports 31 bit addressing, accommodating a larger memory map.

For writes to the BT820, the protocol will operate as in previous EVE revision such as the BT81x, with "WR-Command/Addr3, Addr2, Addr1, Addr0, DataX, DataY, DataZ, ...". The WR-Command is a '1' in the most significant bit in Addr3.

For reads from the BT820, the protocol has updated to "RD-Command/Addr3, Addr2, Addr1, Addr0, (poll for 0x01), 0x01, DataX, DataY, DataZ, ...". The RD-Command is a '0' in the most significant bit in Addr3. The polling period ends when the MCU receives a 0x01 data valid byte, indicating the start of valid data from the next byte onwards.

In SPI Single channel mode, the address and data are transmitted to the BT820 on the MOSI data port during a write transaction as shown in Figure 10.

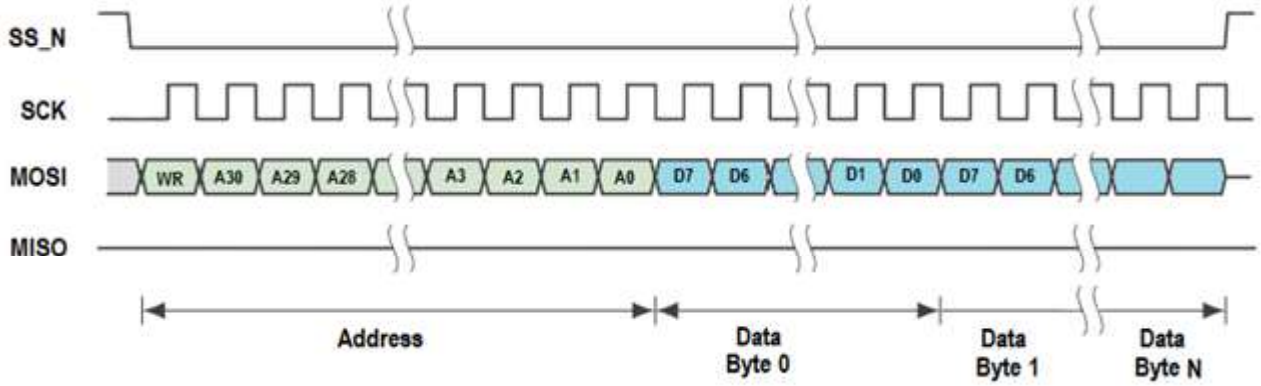


Figure 10 – Write Transaction Using Single Channel Mode

During read transactions the address is transmitted to the BT820 on the MOSI data port and the data is received on the MISO data port as shown in Figure 11. It also shows the polling for 0x01 and the data valid byte before the valid data.

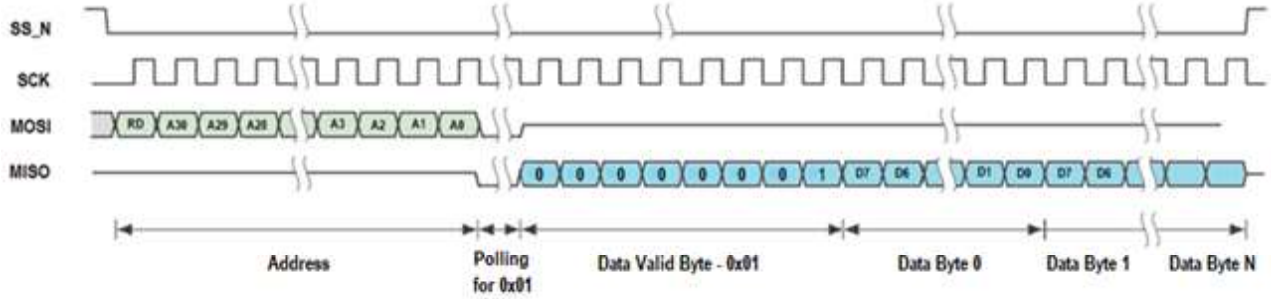


Figure 11 – Read Transaction Using Single Channel Mode

In SPI Dual channel mode, the address and data are transmitted on both the MISO and the MOSI data ports during write transactions with the most significant bit (MSB) transmitted on the MISO data port as shown in Figure 12.

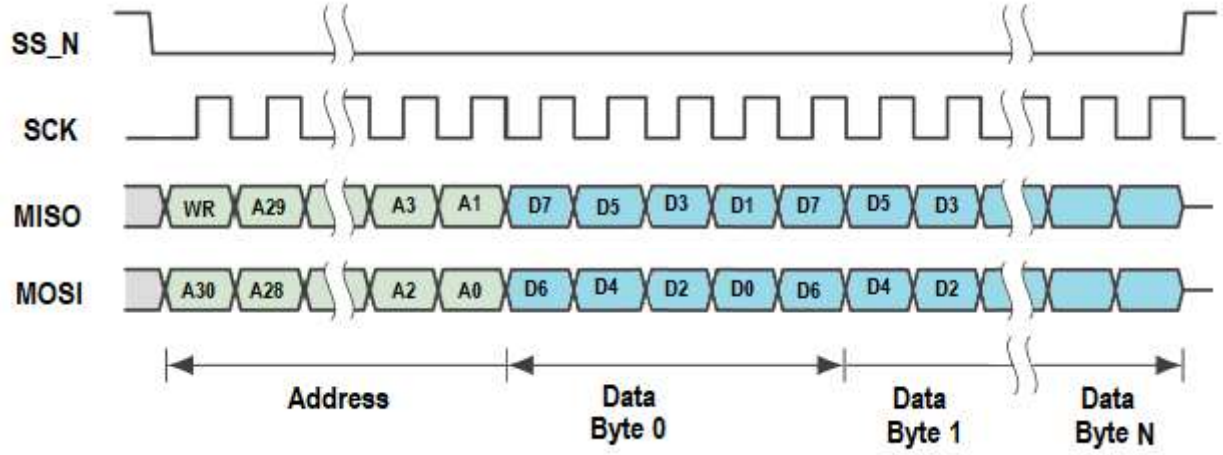


Figure 12 – Write Transaction Using Dual Channel Mode

During read transactions, the MCU changes the data ports to input after the desired address is transmitted and polls for 0x01. Upon receiving 0x01, the next bytes onwards are the valid data bytes as shown in Figure 13.

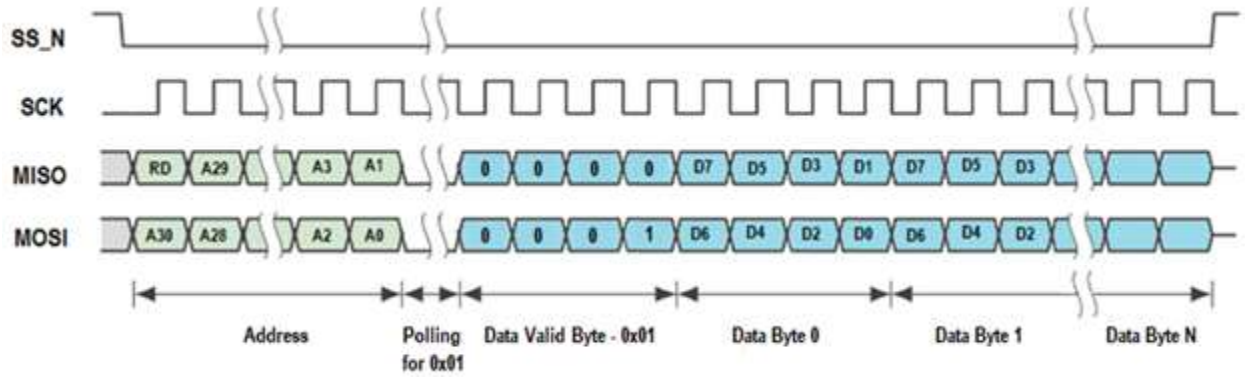


Figure 13 – Read Transaction Using Dual Channel Mode

In SPI Quad channel mode, the transactions are similar to SPI Dual channel mode except for the additional IO3 and IO2 data ports. The address and data are transmitted on IO3, IO2 MISO and MOSI data ports with the most significant bit transmitted on IO3.

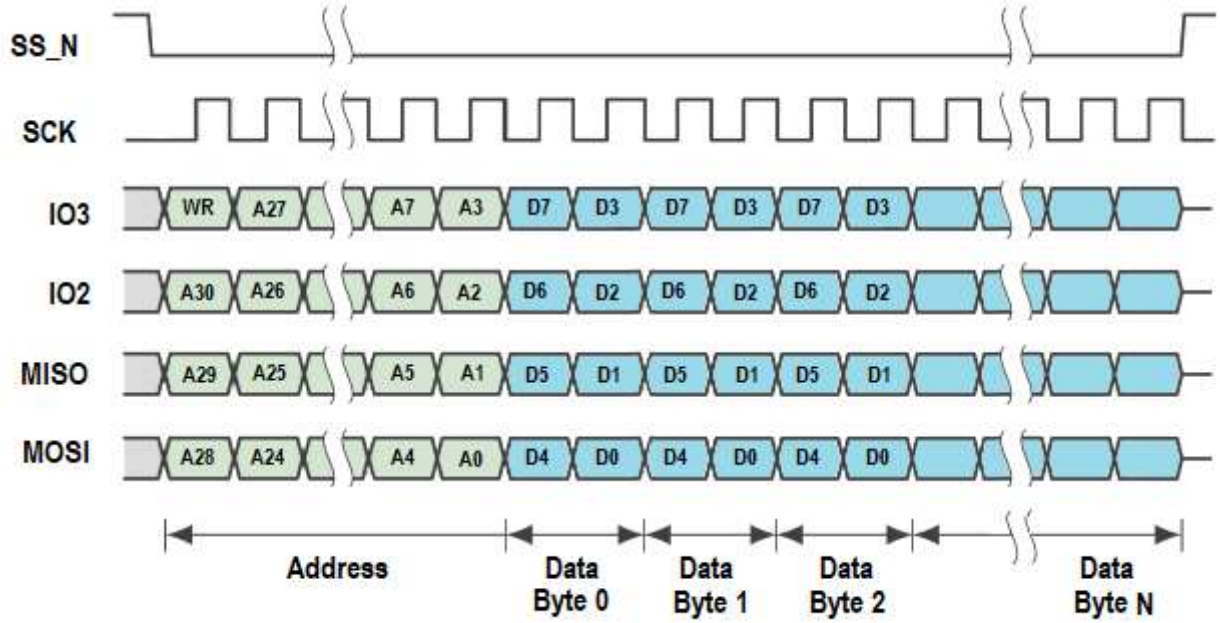


Figure 14 – Write Transaction Using Quad Channel Mode

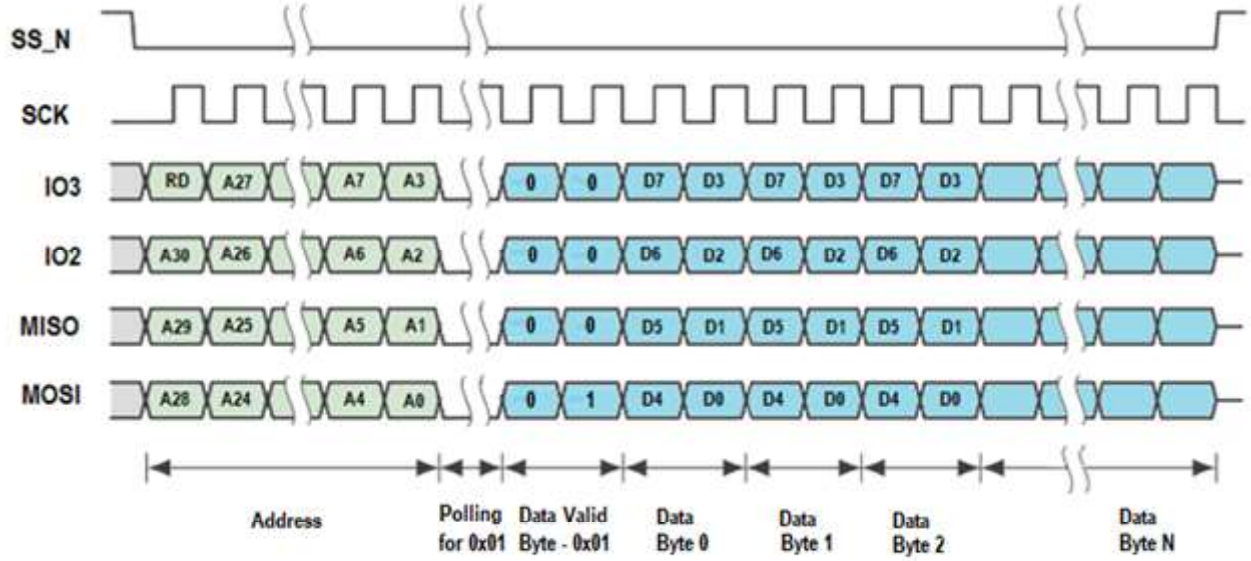


Figure 15 – Read Transaction Using Quad Channel Mode

A transaction is considered to have started when SS_N is driven to logic low and is considered to have ended when SS_N is released to logic high. SS_N high periods between transactions should have a minimum of 2 SCK cycles to ensure proper detection.

The transactions are word based, i.e., the data width must be in blocks of 32 bit when accessing the registers and the DDR memory of the BT820. Addressing to the registers and the DDR memory must also be word aligned, i.e., the last two bits of the received address is ignored.

In the case where the ports are bi-directional, a change of port direction will occur before 0x01 is clocked out of the BT820. Therefore, it is important that the MCU firmware controlling the SPI master changes the SPI master data ports direction to "input" after transmitting Addr0 and start polling for the data valid byte. BT820 will not change the port direction until it starts to clock out the data valid byte. The polling period will be used as a change-over period when neither the SPI master nor BT820 is driving the bus. The data ports must thus have pull-downs.

The QSPI Host Interface will reset all its data ports direction to input mode once SS_N goes inactive.

Note that IO2 and IO3 data pins in the QSPI host interface are shared with GPIO0 and GPIO1. These pins take on the QSPI host interface data pins when it is configured to QSPI Quad channel mode. Otherwise, they default to GPIO0 and GPIO1. The application software might require the QSPI host interface to switch between different channel modes, including Quad channel mode. As the default pin type settings for the GPIOs are input with pull-up, the pin type settings for GPIO0 and GPIO1 should then be set to match the QSPI host interface settings. Leaving them in their default pull-up settings will cause unnecessary power leakage.

4.5.2 Serial Data Protocol

The BT820 appears to the MCU as a memory-mapped SPI device. The MCU communicates with the BT820 using reads and writes to a large (2 Gbytes) address space. Within this address space are dedicated areas for graphics, audio, and touch control. Refer to BRT AN086 BT82X Series Programming Guide for detailed memory map. The MCU reads and writes the BT820 address space using the SPI transactions. Theses transactions are memory read, memory write and command write.

4.5.3 Host Memory Read

For host memory read transactions, the MCU sends the 31 bit address with the MSB sets to '0'. This is followed by polling for the data valid byte. The BT820 responds with the data valid byte followed by valid data bytes.

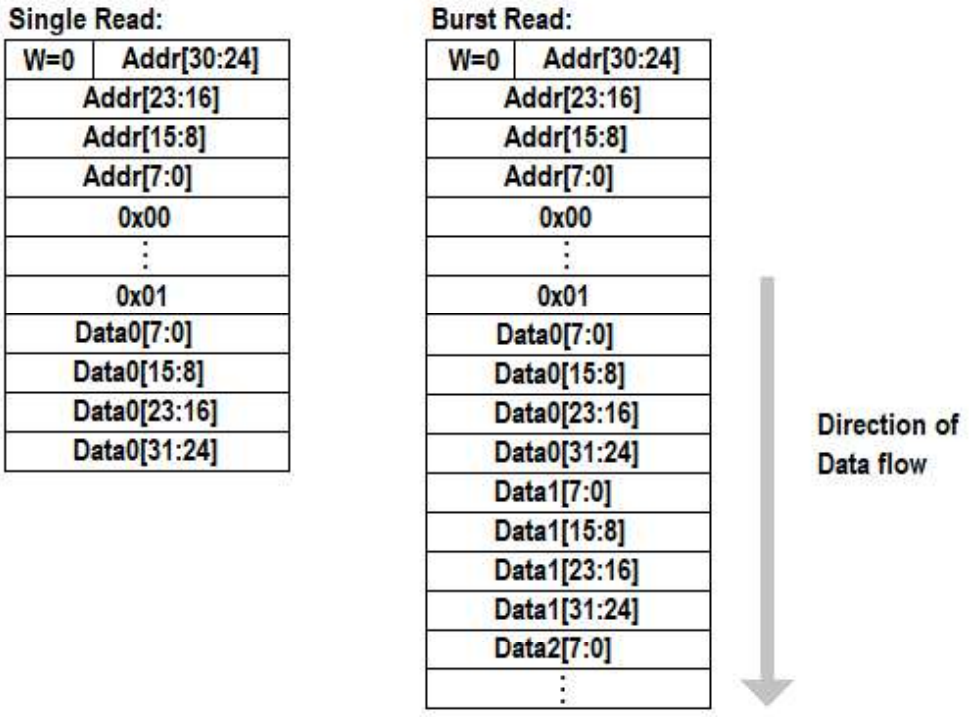


Figure 16 – Host Memory Read Transaction

The BT820 also supports memory burst read to increase the efficiency when accessing the internal registers and memories. The memory burst read are supported only in Single channel mode and Dual channel mode when accessing to the internal registers. Burst read in Quad channel mode is only supported when accessing to the DDR memory.

Figure 16 illustrates the direction of the data flow in a Single read transaction and a burst read transaction. The burst read transaction is enabled by default and can be disabled through register settings in the BT820. Refer to BRT AN086 BT82X Series Programming Guide for details on how to disable the burst read transaction.

When enabled, the BT820 auto-increments the address and pre-fetch the read data. The pre-fetched data is discarded if SS_N is deactivated. In the event where there is an illegal addressing, BT820 will return an error code 0xDEADABBA.

When disabled, the BT820 will return the same data value until the SS_N is deactivated.

4.5.4 Host Memory Write

For host memory write transactions, the MCU sends the 31 bit address with the MSB sets to '1'. This is followed by the desired data to be written.

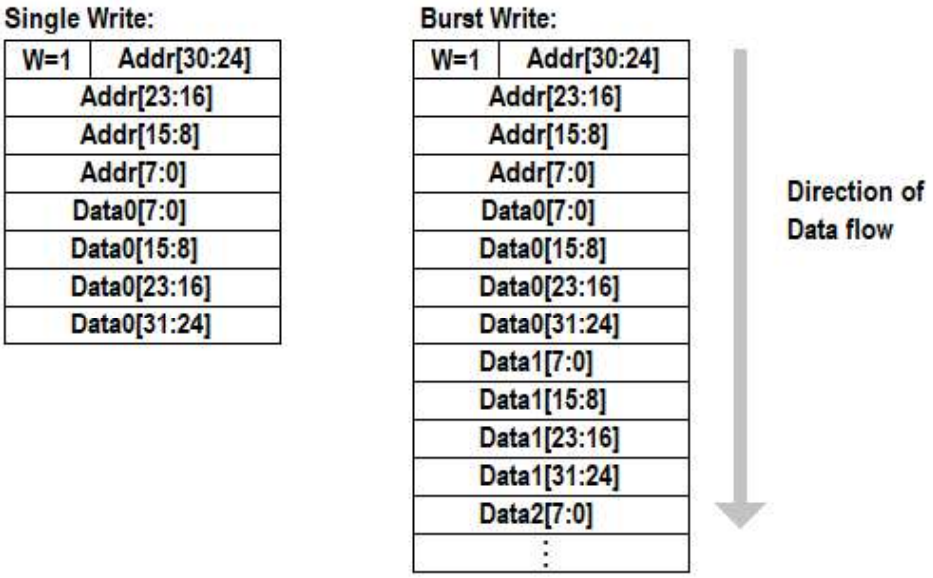


Figure 17 – Host Memory Write Transactions

The BT820 also supports memory burst write transactions. Similar to the burst read, burst writes are supported only in Single channel mode and Dual channel mode when accessing to the internal register. Burst write in Quad channel mode is only supported when accessing to the DDR memory.

Figure 17 illustrates the direction of the data flow in Single write transaction and in a burst write transaction. The burst write transaction is always enabled. The MCU writes data until it deactivates the SS_N. The address is auto-incremented as long as the SS_N is active. The write data is expected to be in blocks of 32-bit. Any incomplete data is discarded when SS_N deactivates.

4.6 Host Commands

BT820 provides a set of host commands for system configurations. The host command can only be executed when the QSPI host interface is operating in Single channel mode. They will be ignored when it is in either Dual or Quad channel modes.

The host command uses a special SPI sequence to program the system configuration. The system configuration registers programmed by the host command should only be updated when the system is in an idle state, i.e., when BT820 is not in ACTIVE state and they retained their settings when the system enters lower power states. These registers are only reset when POR or RST_N pin is activated, or when power is lost.

Byte	
1	0x00 / 0xFF
2	Command
3	Configuration Parameter
4	0x00
5	0x00

Figure 18 – Host Command Transaction

The SPI sequence for the host command is shown in Figure 18.

To write to the system configuration, the MCU sends 0xFF followed by the Command and Configuration parameter of the desired system configuration, and two bytes of trailing '0'.

The ACTIVE Command has a special sequence where the MCU sends 0x00 across all 5 bytes. Refer to section 4.17.4.1 for more information about the ACTIVE command.

Refer to BRT AN086 BT82X Series Programming Guide for detailed descriptions of the host commands.

4.7 Quad SPI Flash Interface

The BT820 implements a Quad SPI (QSPI) Flash Interface that acts as a QSPI master to connect to an external NOR / NAND flash memory device. Application specific graphics assets such as Unicode fonts and images can be stored in the flash memory. The BT820 graphics engine can read these gaphics assets directly and write them to the main memory without going through the external MCU, thus significantly off-loading the MCU from feeding the display contents.

The BT820 supports XIP (execute-in-place) operations and Discoverable Parameters (SFDP) register when using NOR flash. The interface work at the system clock speed in 4-bit mode, providing a maximum data read throughput of 288Mbit/s at 72 MHz system clock.

Figure 19 illustrates a typical connection for Flash Memory device.

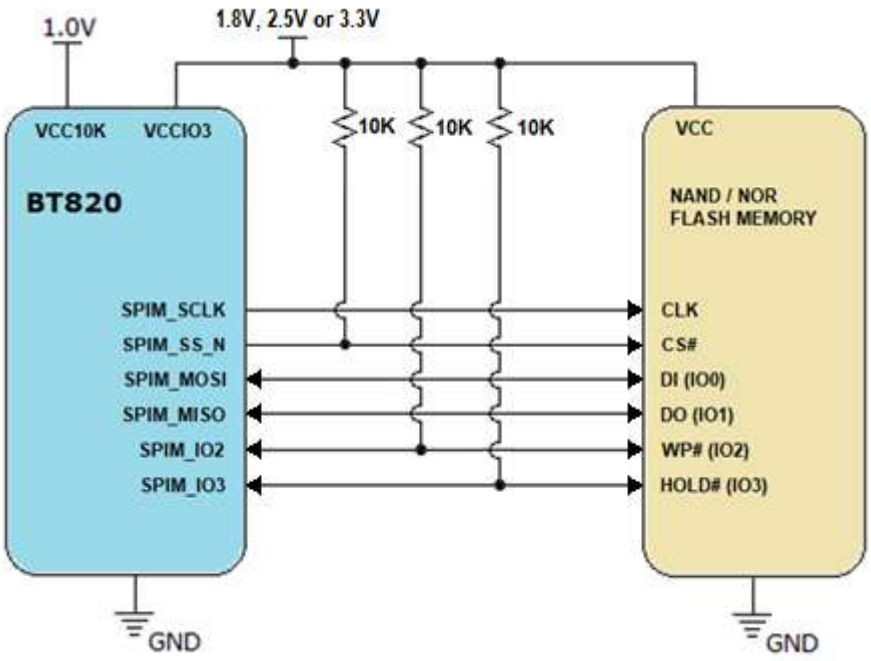


Figure 19 – Typical Connection for Flash Memory

The BT820 supports a separate I/O voltage (VCCIO3) for QSPI flash interface allowing the use of a wider range of flash devices without affecting the other interfaces.

Brand	Model	JEDEC ID	Description
Alliance	AS5F31G04SND-08LIN	52 25 52	3.3V, 1Gbit, QSPI, 120MHz
	AS5F32G04SND-08LIN	52 2E 52	3.3V, 2Gbit, QSPI, 120MHz
	AS5F34G04SND-08LIN	52 2F 52	3.3V, 4Gbit, QSPI, 120MHz
	AS5F38G04SND-08LIN	52 2D 52	3.3V, 8Gbit, QSPI, 120MHz
	AS5F12G04SND-10LIN	52 8E 52	1.8V, 2Gbit QSPI, 100MHz
	AS5F14G04SND-10LIN	52 8F 52	1.8V, 4Gbit, QSPI, 100MHz
	AS5F18G04SND-10LIN	52 8D 52	1.8V, 8Gbit, QSPI, 100MHz
Winbond	W25N01GV series	EF AA 21	3.3V, 1Gbit, QSPI, 104MHz
	W25N01KV series	EF AE 21	3.3V, 1Gbit, QSPI, 104MHz
Micron	MT29F2G01ABBGDWB	2C 25 2C	1.8V, 2Gbit, QSPI, 83MHz

Table 6 – Supported NAND Flash Devices

Table 6 lists the supported NAND Flash devices. Note that these are the only NAND flash devices that are supported by BT820.

Brand	Model	Type	Description
Winbond	W25Q128JV series	NOR	IC NOR Flash, 3.3V, 128Mbit, QSPI, 133MHz
Micron	M25QL128 series	NOR	IC NOR Flash, 3.3V, 128Mbit, QSPI, 133MHz
Micronix	MX25L256 series	NOR	IC NOR FLASH, 3.3V, 256Mbit, QSPI, 120MHz
ISSI	IS25LP256	NOR	IC NOR FLASH, 3.3V, 256Mbit, QSPI, 133MHz

Table 7 – Supported NOR Flash Devices

Table 7 lists the supported NOR Flash Devices. The devices listed in Table 7 represent samples for each family test compatible with BT820.

In certain flash memory device such as the W25N01GVZEIG from Winbond, the HOLD# and IO3 signals share the same pin, as to the WP# and IO2 signals. During Quad operations, the HOLD# pin functions as a data I/O pin, temporarily disabling the hold function until the operation completes. Therefore, an external pull-up resistor is necessary to prevent the HOLD# pin from floating.

4.8 SD Card Host Controller

The BT820 implements a SD Card Host Controller offering access to external large capacity non-volatile memory. The SD Card host controller operates up to 36MHz and supports DDR50 and SDR50 SD modes. It is powered by VCCIO4, which can be configured to 1.8V for low voltage signalling without affecting the other interfaces.

Figure 20 illustrates a typical connection for the SD Host controller.

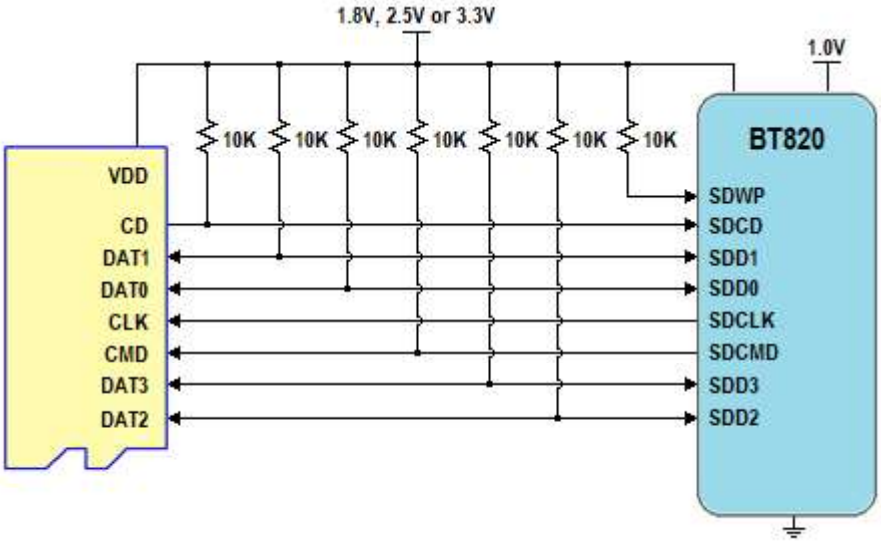


Figure 20 – Typical connection for SD Host Controller

4.9 Touch Engine and Interface

The BT820 is compatible with various touch controllers, including capacitive touch controller ICs from FocalTech, Goodix, Ilitek and Sitronix, as well as resistive touch controller ICs from TI and Microchip.

The Touch Engine of the BT820 communicates with the external touch device through an I2C interface. The I2C interface supports standard mode, up to 100KHz and fast mode, up to 400KHz. The Touch Engine supports auto-discovery of the attached external touch devices. Up to 5 touches can be reported and stored in the BT820 registers.

Figure 21 illustrates the typical Touch Screen Connection.

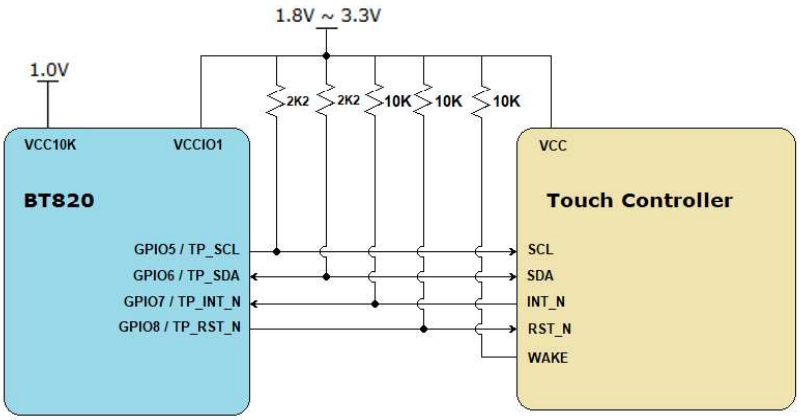


Figure 21 – Typical Touch Screen connection

Note that the touch interface of BT820 is powered by VCCIO1 that also powered by QSPI Host Interface. Level shifters are required if the voltage level of the external touch panel does not match the MCU's I/O voltage.

Table 8 lists the capacitive touch controllers and Table 9 lsts the resistive touch controllers which are supported by BT820 auto-discovery feature. Note that the particular models listed in this table represent samples for each family tested compatible with BT820. Other models not listed are expected to work if their protocol is compatible to the listed controller.

Brand	Models	I2C Address
FocalTech	FT5x06 series: FT5206, FT5306, FT5406	0x38
	FT5x16 series: FT5316	
	FT5x26 series: FT5426	
	FT5x36 series:	
	FT5x46 series:	
Goodix	GT9xx series:	0x5D
Ilitek	ILI2511	0x41
Sitronix	ST1633i	0x55

Table 8 – List of Supported Capacitive Touch Controller

Brand	Models	I2C Address
Microchip	AR1021	0x4D
TI	TSC2007	0x48

Table 9 – List of Supported Resistive Touch Controller

4.10 Audio Engine

The Audio Engine of the BT820 outputs stereo audio from two audio sources; sound synthesizer and audio file playback.

4.10.1 Sound Synthesizer

BT820 provides a sound processor that generates the sound effects from a small library of wavetables which are stored in the ROM. Table 10 lists the supported sound effects and Table 11 lists the supported MIDI note effects. Sound effect marked with a 'Y' in the Continuous column will play on a loop until they are either interrupted or instructed to switch to the next sound effect.

For sound effect marked with a 'Y' in the Pitch Adjust column, the MIDI note effect is combined with the sound effect to change the pitch of the sound effect.

Refer to BRT AN086 BT82X Series Programming Guide for details on how to play a sound effect.

Value	Effect	Continuous	Pitch Adjust
0x00	Silence	Y	N
0x01	Square wave	Y	Y
0x02	Sine wave	Y	Y
0x03	Sawtooth wave	Y	Y
0x04	Triangle wave	Y	Y
0x05	Beeping	Y	Y
0x06	Alarm	Y	Y
0x07	Warble	Y	Y
0x08	Carousel	Y	Y
0x10	1 short pips	N	Y
0x11	2 short pips	N	Y
0x12	3 short pips	N	Y
0x13	4 short pips	N	Y
0x14	5 short pips	N	Y
0x15	6 short pips	N	Y
0x16	7 short pips	N	Y
0x17	8 short pips	N	Y
0x18	9 short pips	N	Y
0x19	10 short pips	N	Y
0x1A	11 short pips	N	Y
0x1B	12 short pips	N	Y
0x1C	13 short pips	N	Y
0x1D	14 short pips	N	Y
0x1E	15 short pips	N	Y
0x1F	16 short pips	N	Y
0x23	DTMF #	Y	N
0x2C	DTMF *	Y	N
0x30	DTMF 0	Y	N
0x31	DTMF 1	Y	N

Value	Effect	Continuous	Pitch Adjust
0x32	DTMF 2	Y	N
0x33	DTMF 3	Y	N
0x34	DTMF 4	Y	N
0x35	DTMF 5	Y	N
0x36	DTMF 6	Y	N
0x37	DTMF 7	Y	N
0x38	DTMF 8	Y	N
0x39	DTMF 9	Y	N
0x40	Harp	N	Y
0x41	Xylophone	N	Y
0x42	Tuba	N	Y
0x43	Glockenspiel	N	Y
0x44	Organ	N	Y
0x45	Trumpet	N	Y
0x46	Piano	N	Y
0x47	Chimes	N	Y
0x48	Music box	N	Y
0x49	Bell	N	Y
0x50	Click	N	N
0x51	Switch	N	N
0x52	Cowbell	N	N
0x53	Notch	N	N
0x54	Hihat	N	N
0x55	Kickdrum	N	N
0x56	Pop	N	N
0x57	Clack	N	N
0x58	Chack	N	N
0x60	Mute	N	N
0x61	unmute	N	N

Table 10 – Sound Effects

MIDI note	ANSI note	Freq (Hz)
21	A0	27.5
22	A#0	29.1
23	B0	30.9
24	C1	32.7
25	C#1	34.6
26	D1	36.7
27	D#1	38.9
28	E1	41.2
29	F1	43.7
30	F#1	46.2
31	G1	49.0
32	G#1	51.9
33	A1	55.0
34	A#1	58.3
35	B1	61.7
36	C2	65.4
37	C#2	69.3
38	D2	73.4
39	D#2	77.8
40	E2	82.4
41	F2	87.3
42	F#2	92.5
43	G2	98.0
44	G#2	103.8
45	A2	110.0

MIDI note	ANSI note	Freq (Hz)
65	F4	349.2
66	F#4	370.0
67	G4	392.0
68	G#4	415.3
69	A4	440.0
70	A#4	466.2
71	B4	493.9
72	C5	523.3
73	C#5	554.4
74	D5	587.3
75	D#5	622.3
76	E5	659.3
77	F5	698.5
78	F#5	740.0
79	G5	784.0
80	G#5	830.6
81	A5	880.0
82	A#5	932.3
83	B5	987.8
84	C6	1046.5
85	C#6	1108.7
86	D6	1174.7
87	D#6	1244.5
88	E6	1318.5
89	F6	1396.9

MIDI note	ANSI note	Freq (Hz)
46	A#2	116.5
47	B2	123.5
48	C3	130.8
49	C#3	138.6
50	D3	146.8
51	D#3	155.6
52	E3	164.8
53	F3	174.6
54	F#3	185.0
55	G3	196.0
56	G#3	207.7
57	A3	220.0
58	A#3	233.1
59	B3	246.9
60	C4	261.6
61	C#4	277.2
62	D4	293.7
63	D#4	311.1
64	E4	329.6

MIDI note	ANSI note	Freq (Hz)
90	F#6	1480.
91	G6	1568.0
92	G#6	1661.2
93	A6	1760.0
94	A#6	1864.7
95	B6	1975.5
96	C7	2093.0
97	C#7	2217.5
98	D7	2349.3
99	D#7	2489.0
100	E7	2637.0
101	F7	2793.8
102	F#7	2960.0
103	G7	3136.0
104	G#7	3322.4
105	A7	3520.0
106	A#7	3729.3
107	B7	3951.1
108	C8	4186.0

Table 11 – MIDI Note Effects

4.10.2 Audio Playback

The BT820 can playback audio through its audio outputs. The audio files can be stored in the flash memory device, SD Card memory device or written directly into the DDR memory by the MCU. The Audio Engine picks up the sound samples and outputs them to the corresponding audio outputs.

The audio formats supported by BT820 are listed in Table 12.

Audio Formats	Descriptions
Linear	8-bits MONO PCM
µLAW	8-bits MONO PCM with µLAW algorithm
ADPCM	4-bits MONO IMA Adaptive Differential PCM
S16	16-bits MONO PCM
S16S	16-bits Stereo PCM

Table 12 – Supported Audio Formats

The Audio Engine duplicates the sound samples to the left and right channels when playback in Linear, µLAW, ADPCM and S16 audio formats. When playback in S16S audio format, the left audio data is played to the left channel and the right audio data is played to the right channel.

BT820 supports PCM with 16-bit resolution only.

The supported sample rates (fs) for Linear, S16, S16S are 8KHz, 16KHz, 22.05KHz, 32KHz, 44.1KHz and 48KHz.

The BT820 does not support µLAW and ADPCM audio format for regular audio playback. It only supports the µLAW audio format when playing videos with µLAW encoded audio, and similarly, it only supports the ADPCM audio format when playing videos with ADPCM audio encoded audio.

4.10.2.1 Audio Data

Each sample for Linear audio format and µLAW audio format is a signed byte. For ADPCM, each sample is 4 bits. Hence each byte contains two samples. The first sample is in bits [3:0] and the second sample is in bits [7:4]. For S16, each sample is a signed little-endian 16-bit value. For S16S, each sample is a pair of signed little-endian 16-bit value with the left channel in the lower byte and the right channel in the upper byte.

4.11 Audio Outputs / Interface

BT820 can output audio to either the Stereo Audio output ports in PWM format or Delta-Sigma format, or to the I2S interface in PCM formats. BT820 does not support the use of both Stereo Audio output ports and I2S interface at the same time.

4.11.1 Stereo Audio Output Ports

The stereo audio output ports are implemented using Delta-Sigma encoding through digital output pins, AUDIO_L and AUDIO_R. These are allowed to be configured as PWM encoding at lower carrier frequencies. Refer to section 5.4.6.1 for timing of the carrier frequencies. The stereo audio output ports can be disabled, stopping the carrier frequency when not in use. For details on how to disable the stereo audio output ports, refer to the BRT AN086 BT82x Series Programming Guide.

4.11.2 I2S Interface

The I2S interface only supports transmission in slave mode. The audio formats supported are left-justified, Right-Justified and I2S mode.

The I2S interface for BT820 consists of 3 pins as shown in Table 13.

Pin	Type	Description
I2S_BCLK	Input	I2S bit clock
I2S_LRCLK	Input	I2S left/right clock
I2S_SDAO	Output	I2S serial data output

Table 13 – I2S Interface Digital Pins

The I2S_BCLK pin receives the I2S_BCLK clock signal produced by an external I2S master device, ensuring data synchronization between the master device and the BT820. The BT820 can handle I2S_BCLK frequencies that are 32 times the audio sample frequency (32fs) or 64 times the audio frequency (64fs).

The master device also generates the I2S_LRCLK clock signal to the I2S_LRCLK pin, which specifies the left and right channel data. The frequency of this signal matches the audio sample frequency.

The I2S_SDAO pin transmits the actual audio data from BT82x to the external I2S master device.

Refer to BRT AN086 BT82X Series Programming Guide for details on how to program the I2S interface.

4.11.2.1 Left-Justified Audio Format

In Left-Justified audio format, the most significant bit (MSB) of the audio data is aligned with the start of the frame sync signal. The I2S_LRCLK signal indicates the left channel when it is high and the right channel when itis low.

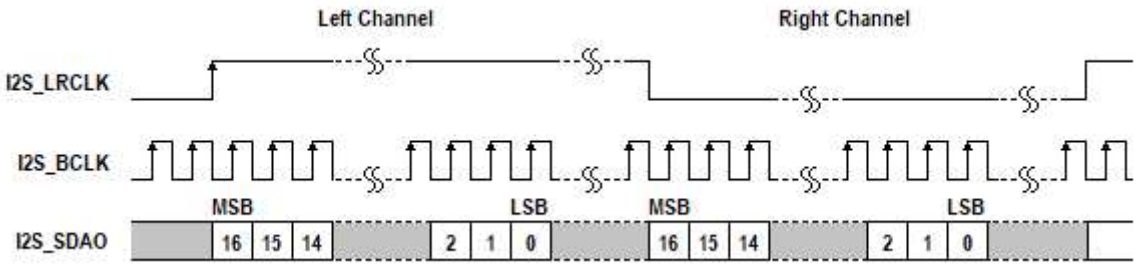


Figure 22 – Left-Justified Audio Format

4.11.2.2 Right-Justified Audio Format

In Right-Justified audio format, the least significant bit (LSB) of the audio data is aligned with the end of the frame sync signal. To align the audio data, dummy bits are inserted onto the I2S_SDAO before the start of the audio data. The number of dummy bits to insert is programmable through internal register of BT820.

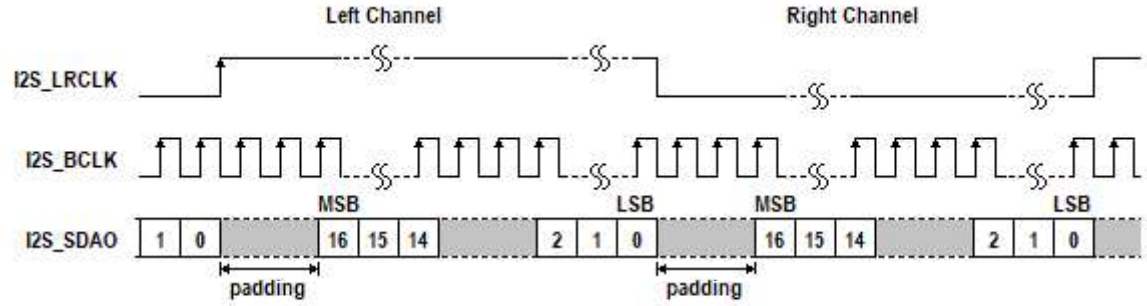


Figure 23 – Right-Justified Audio Format

4.11.2.3 I2S Mode Audio Format

In I2S mode audio format, the most significant bit (MSB) of the audio data is delayed by one bit clock cycle (I2S_BCLK) relative to the I2S_LRCLK signal. The I2S_LRCLK signal indicates the left channel when it is low and the right channel when it is high.

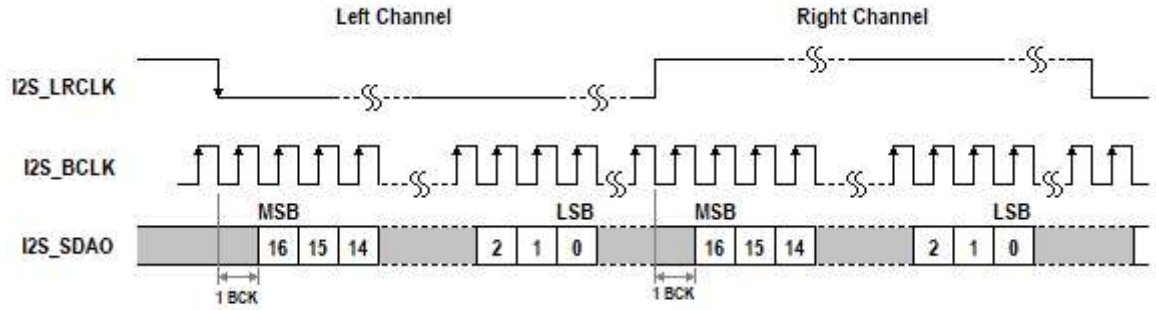


Figure 24 – I2S Mode Audio Format

4.12 Watchdog Timer (WDT)

The watchdog timer uses a 32-bit counter and is driven by the system clock. Hence, at default system clock of 72 MHz, the maximum timeout period supported is 59.6s.

The watchdog timer begins and resets as it count down from a user-defined initial value. Upon reaching a count value of zero, the watchdog timer generates a system reset. The timer needs to be periodically reset to the initial value to prevent the system reset from happening. The countdown can only be stopped by issuing a stop timer.

Refer to BRT AN086 BT82X Series Programming Guide for details on how to program the Watchdog Timer.

4.13 System Clock

4.13.1 Clock Source

The BT820 supports the use of an external 38.4MHz crystal as a clock source for the system clock

Figure 25 shows the pin connections for the crystal.

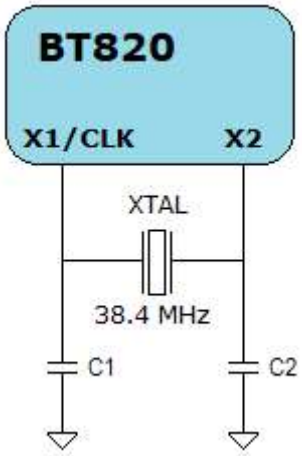


Figure 25 – Crystal Oscillator Connection

An external 38.4 MHz clock source can also be fed to X1 pin directly instead of using a crystal. In this case, the X2 pin is left floating.

4.13.2 Phase Locked Loop

There are 4 Phase Locked Loops (PLLs) inside the chip; the system PLL (PLL1), LVDSPLL (PLL2), DDRPLL (PLL3) and the DDR PHYPLL (PLL4)

The system PLL takes the input clock from the oscillator and generates the system clock and LVDSTX clock.

The LVDSPLL generates the LVDS fast clock from the LVDSTX clock.

The DDRPLL and the DDR PHYPLL are used to generate clock for the DDR module.

4.13.3 Clock Enable

Upon power-on, the BT820 is in sleep mode. The system clock will enabled when the MCU activates the system via host commands. Refer to section 4.6 for details on Host Commands

4.13.4 Clock Frequency

By default, the system clock is running at 72 MHz when the input clock is at 38.4 MHz. The system clock can be programmed to other frequencies through host command

Refer to BRT AN086 BT82X Series Programming Guide on how to program the system clock.

4.14 Interrupt

The BT820 provides an active-low interrupt output pin, INT_N, to the MCU. The INT_N pin can be configured as an open drain output or push-pull output. It is configured as an open-drain output by default.

When BT820 is active, the INT_N is driven low whenever an event occurs in the interrupt source, as long as the interrupt source for that event is unmasked and the interrupt enable is activated. Additionally, the interrupt flag for that event is set to indicate the cause of the interrupt.

The INT_N signal is realeased or driven high only when the interrupt flags for all events are cleared.
When the BT820 is in a lower power state, the interrupt source is routed to the interrupt signal from GPIO7. This setup enables a touch-screen panel to generate an interrupt directly to the MCU, allowing the MCU to wake up the BT820 from its low power state.

Refer to BRT AN086 BT82X Series Programming Guide for detailed descriptions on the interrupt sources.

4.15 General Purpose IO (GPIO) Pins

The BT820 can be set up to utilize up to 16 GPIO pins. These pins are powered by various VCCIO voltages, and some of the GPIO pins have alternate functions. Table 14 lists the GPIO pins along with their corresponding VCCIO voltages and their alternate functions.

Pin	I/O Voltage	Alternate Function
GPIO[15:9]	VCCIO2	None
GPIO8	VCCIO1	TP_RST_N
GPIO7	VCCIO1	TP_INT_N
GPIO6	VCCIO1	TP_SDA
GPIO5	VCCIO1	TP_SCL
GPIO[4:2]	VCCIO1	None
GPIO1	VCCIO1	IO3
GPIO0	VCCIO1	IO2

Table 14 – GPIO Pins

4.16 Miscellaneous Control

4.16.1 Backlight Control Pin

The backlight dimming control pin (BACKLIGHT) is a Pulse-Width Modulation (PWM) signal. Backlight dimming can be controlled from this pin by specifying the output frequency and the duty cycle of the PWM signal.

The PWM output has a frequency range of 250Hz to 10KHz.

4.16.2 DISP Control Pin

The DISP pin is a general-purpose output that can be used to enable or reset the LCD display panel.

4.17 Power Management

4.17.1 Power Supply

The BT820 may operate using a single supply of 3.3V applied to VCC33A and VCCIO pins.

For operation with an MCU at a lower supply voltage, connect VCCIO1 to the MCU I/O supply voltage to match the interface voltage. This will also affect the I/O supply voltage to the Touch Controller as the Touch Interface is also using the same VCCIO1 IO supply voltage.

The Display, I2S interface and Audio I/O uses VCCIO2 which is fixed at 3.3V.

QSPI Flash Interface uses VCCIO3 which should match or share the I/O supply voltage of the NOR / NAND flash memory device.

The SD Card Host Controller uses VCCIO4 which should match or share the I/O supply voltage of the external SD Card.

Symbol	Typical	Description
VCCIO1	1.8V, or 2.5V, or 3.3V	Supply for Host interface digital I/O pins Supply for the GPIO I/O pins for Touch Control
VCCIO2	3.3V	Supply for Display, I2S and audio I/O pins
VCCIO3	1.8V, or 2.5V, or 3.3V	Supply for SPIM I/O pins
VCCIO4	1.8V, or 2.5V, or 3.3V	Supply for SD interface I/O pins
VCC33A_REG	3.3V	Power supply to internal regulator
VCC10A_REG	1.0V	Power supply generated by internal regulator
VCC10K	1.0V	Digital core power supply
VCC33A_LVDSTX	3.3V	LVDS TX analog supply
VCC10_DDR	1.0V	Digital core supply for DDR PHY
VCCIO_DDR	1.5V, or 1.35V, or 1.2V	Digital IO supply for DDR PHY
VCCIO_DDR_CK	1.5V, or 1.35V, or 1.2V	Power supply for CKE, CK and CKB of DDR interface
VCC33A_OSC	3.3V	Power supply for OSC
VCC33A_OTP	3.3V	Power supply for OTP
VCC10A_PLL1 VCC10A_PLL2 VCC10A_PLL3 VCC10A_PLL4	1.0V	Power supply for PLL

Table 15 – Power Supplies

Note: VCCIO_DDR and VCCIO_DDR_CK should be 1.5V for DDR3 or 1.35V for DDR3L or 1.2V for LPDDR2.

4.17.2 Internal Regulator and POR

The internal regulator outputs 1.0V (VCC10A_REG) to supply power to the core circuit from the 3.3V (VCC33A_REG) input. It is recommended to connect a 47uF capacitor between VCC33A_REG and GND to reduce power noise. This capacitor should be placed near the VCC33A_REG pins.

The internal regulator requires a compensation capacitor (minimum 3.3uF) to be stable. A typical design uses a 4.7uF or 10uF capacitor between the VCC10A_REG and GND pins. This capacitor should be placed near the VCC10A_REG pins. Do not connect any other load to the VCC10A_REG pins.

The internal POR will generate a Power-On-Reset (POR) pulse when the output voltage rises above the POR threshold. The POR wll reset all the core digital circuits.

4.17.3 Reset and Boot-up Sequence

BT820 provide a RST_N pin for global reset. This has the same reset targets as the POR.

The RST_N pin can be connected to a GPIO of an external MCU for hardware reset function. The external MCU must hold the RST_N pin low for a minimum of 214μs to trigger a chip wide reset. Alternatively, it can be pulled up to VCCIO1 through a 47KΩ-0.1μF (RC) network to ensure a system reset after the power supplies are stable.

Table 16 list the power groupings for the BT820 input voltage.

Power Blocks	Power
Group 1	VCCIO1, VCCIO2 (3.3V only), VCCIO3, VCCIO4

Group 2	VCC33A_REG, VCC33A_OSC, VCC33A_OTP, VCC33A_LVDSTX, VCC33A_LVDSRX
Group 3	VCCIO_DDR, VCCIO_DDR_CK
Group 4	VCC10K, VCC10A_DDR, VCC10A_LVDSRX, VCC10A_PLL1, VCC10A_PLL2, VCC10A_PLL3, VCC10A_PLL4

Table 16 – Power Grouping

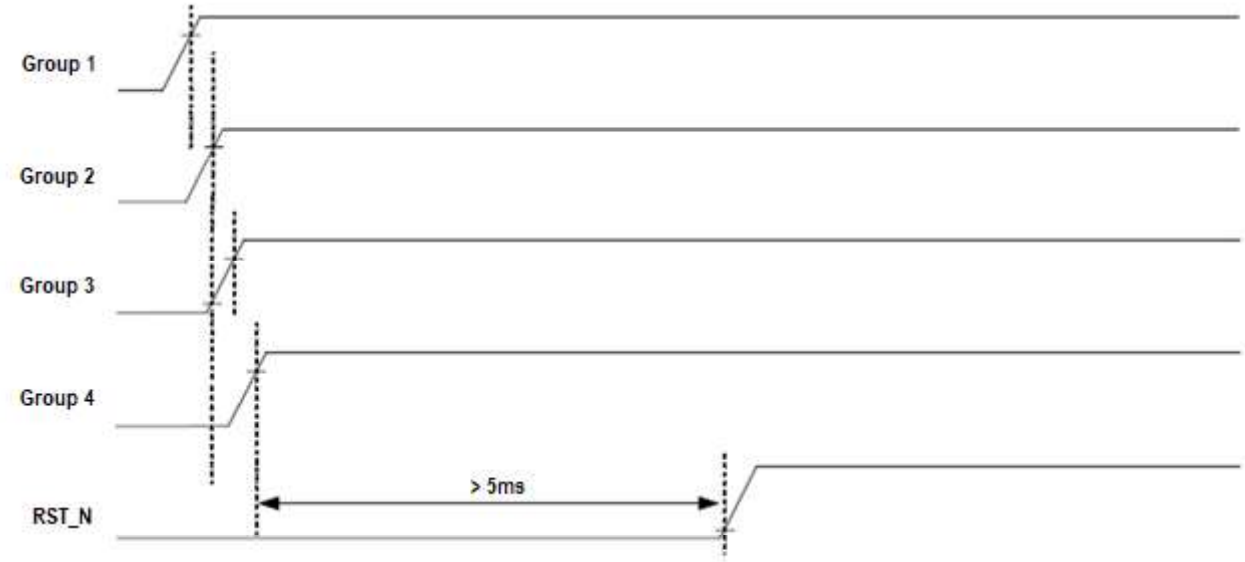


Figure 26 – Power up and reset sequence using RC Network

Figure 26 shows the power up and reset sequence using the RC network. The power rails from Group 1 must be powered up before or at the same time as those from Group 2. Since VCC33A_REG powers up VCC10A_REG, which in turns powers up Group 4, the power rails from Group 3 need to be powered up after or simultaneously with Group 2 before Group 4.

When the power rails from Group 4 are powered up by an external power source, they must be powered up after all other groups have been powered up.

The RST_N signal must be de-asserted at least 5ms after the power rails from Group 4 have powered up.

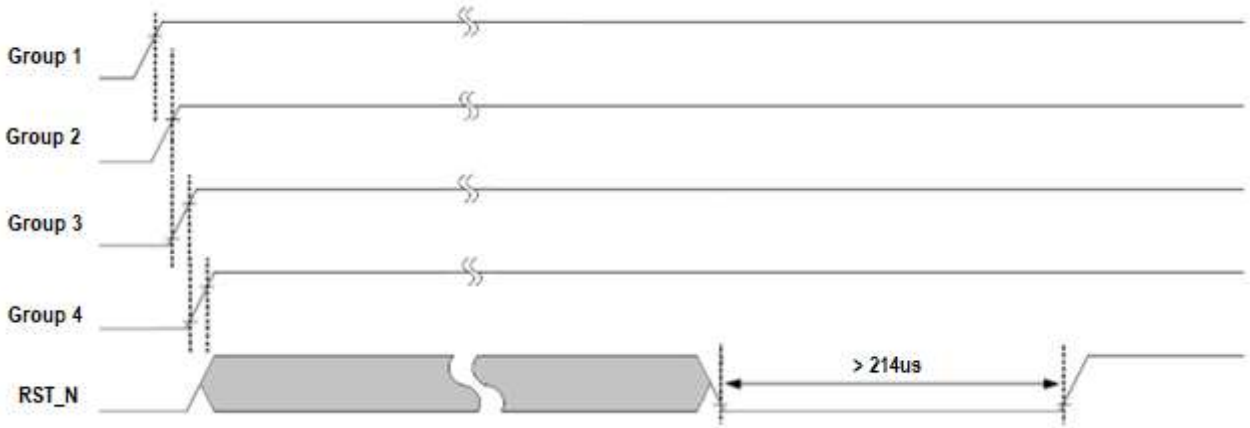


Figure 27 – Power up and reset sequence using MCU

Figure 27 shows the power up sequence where the RST_N signal is controlled by the MCU. The MCU must hold the RST_N signal low for a minimum of 214us before releasing the reset.

4.17.4 Power Modes

When the supplies to VCCIO and VCC33A are applied, the internal regulator is powered by VCC33A_REG. An internal POR pulse will be generated when the output voltage rises above the POR threshold and the oscillator will be available after a masked period. After the RST_N is released and power up initialization has completed. The BT820 will stay in the SLEEP state.

When needed, the MCU can set the BT820 to ACTIVE state by performing an ACTIVE command using the host command. The graphics engine, audio engine and touch engine are only functional in the ACTIVE state. To save power, the MCU can send a command to put the BT820 into any of the low power states: STANDBY, SLEEP and POWERDOWN.

Refer to BRT AN086 BT82X Series Programming Guide for detailed sequence on entering and exiting low power states.

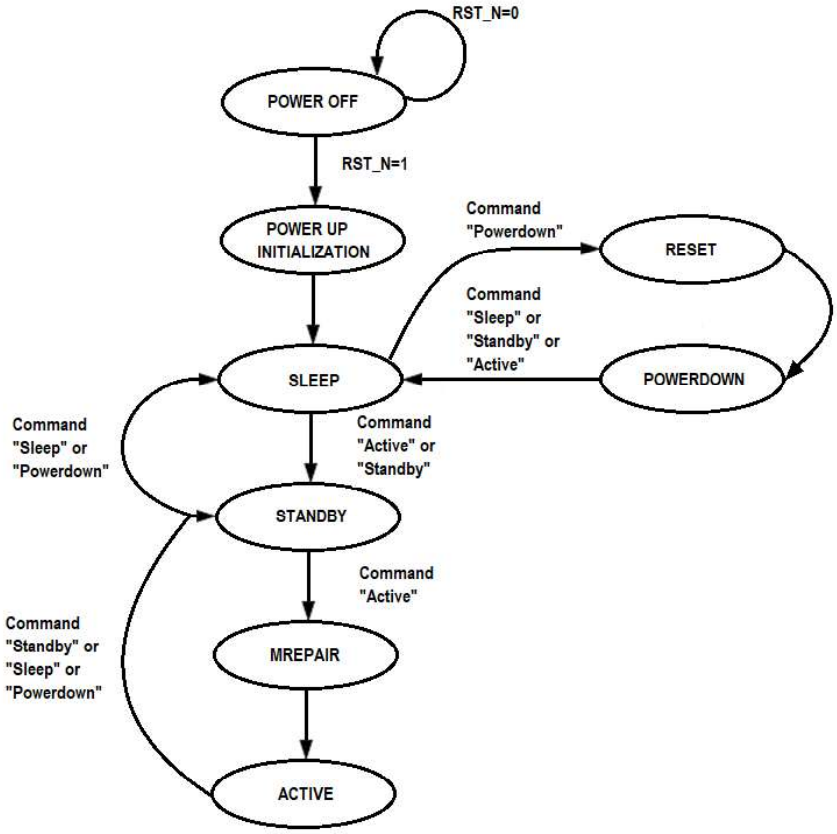


Figure 28 – Power State Transition

4.17.4.1 ACTIVE State

In ACTIVE state, the BT820 is fully operational.

4.17.4.2 STANDBY State

In STANDBY state, the DDR controller puts the DRAM into its active power-down mode after a period of inactivity. The system clock to the core engines is disabled. All registers contents are retained.

4.17.4.3 SLEEP State

In SLEEP state, the DDR DRAM is put into self-refresh mode. The DDR interface and the PLLs are disabled. The system clock to the core engines is disabled. All registers contents are retained.

4.17.4.4 POWERDOWN State

In POWERDOWN state, the core engines are held in reset state and their power supplies are turned off. The QSPI host interface remains functional. The contents for all registers, except for the Top-Level System Registers, are lost and reset to their default settings. The internal regulator remains on.

4.17.5 Power up Default Pin State

The QSPI Host Interface pins, GPIO pins, Stereo Audio output pins, Backlight control pin, DISP pin, interrupt pin, I2S interface pins, SD Card interface pins, and QSPI Master Interface pins supports different drive strength currents, slew rate and pin states through the programming of internal registers of the BT820.

Table 17 lists the power up default configuration states of the pins.

Pin Name	Pin State when RST_N is Active	Default Configuration		
		Pull-up / Pull-Down	Slew Rate	Drive Strength
SCK	In	None	-	-
SS_N	In	None	-	-
MISO	Float	None	-	-
MOSI	In	None	-	-
GPIO0/IO2	In	GPIO0: Pull-up	-	-
GPIO1/IO3	In	GPIO1: Pull-up	-	-
INT_N	OD	-	-	-
RST_N	In	None	-	-
SPIM_SCLK	In	Pull-up	-	-
SPIM_SS_N	In	Pull-up	-	-
SPIM_MISO	In	Pull-up	-	-
SPIM_MOSI	In	Pull-up	-	-
SPIM_IO2	In	Pull-up	-	-
SPIM_IO3	In	Pull-up	-	-
SDCD	In	Pull-up	-	-
SDCLK	Out	-	Slow	DSD1
SDCMD	In	Pull-up	-	-
SDWP	In	Pull-up	-	-
SDD0	In	Pull-up	-	-
SDD1	In	Pull-up	-	-
SDD2	In	Pull-up	-	-
SDD3	In	Pull-up	-	-
DISP	OUT	-	Fast	DSD1
BACKLIGHT	OUT	-	Fast	DSD1
GPIO3	In	Pull-up	-	-
GPIO4	In	Pull-up	-	-
GPIO5 / TP_SCL	In	Pull-up	-	-
GPIO6 / TP_SDA	In	Pull-up	-	-
GPIO7 / TP_INT_N	In	Pull-up	-	-
GPIO8 / TP_RST_N	In	Pull-up	-	-
AUDIO_L	OUT	-	Slow	DSD4
AUDIO_R	OUT	-	Slow	DSD4
I2S_BCLK	In	None	-	-
I2S_LRCLK	In	None	-	-
I2S_SDAO	OUT	-	Slow	DSD1
GPIO2	In	Pull-up	-	-
GPIO9 / TIO3	In	Pull-up	-	-
GPIO10 / TIO4	In	Pull-up	-	-
GPIO11 / TIO5	In	Pull-up	-	-
GPIO12 / TIO6	In	Pull-up	-	-
GPIO13 / TIO7	In	Pull-up	-	-
GPIO14 / TIO8	In	Pull-up	-	-
GPIO15 / TIO9	In	Pull-up	-	-

Table 17 – Default Configuration of Digital Pins

4.17.6 Drive Strength

The drive strength varies according to the programming of internal registers in the BT820 and the VCCIO that is supplied to the pin. BT820 supports 4 different drive strength settings, DSD1, DSD2, DSD3 and DSD4.

Table 18 lists the drive strength of each setting at different VCCIO levels.

VCCIO	DSD1	DSD2	DSD3	DSD4	Unit
3.3V	12.5	15	17.5	20	mA
2.5V	10	12	14	16	mA
1.8V	6	7.2	8.4	9.6	mA

Table 18 – Digital Output Pin Drive Strength

4.17.7 Slew Rate

BT820 supports fast and slow slew rate for the digital pins.

4.17.8 Pin state

Each digital pin can be configured to float, pull down, pull up or keep last value.

4.18 Pin Status at Different Power States

The BT820 pin status depends on the power state of the chip. At the power transition from ACTIVE to STANDBY or ACTIVE to SLEEP, all pins retain their previous status. Software needs to disable the LVDSTX and LVDSRX, disable the I2S interface, and set Stereo Audio Outputs, and BACKLIGHT to a known state before issuing power transition commands.

Table 19 lists the pin status in each power states.

Pin Name	Pin Status at Different Power States				
	System Reset	ACTIVE	STANDBY	SLEEP	POWERDOWN
SCK	In	In	In	In	In
SS_N	In	In	In	In	In
MISO	Float	I/O	I/O	I/O	SS_N=1: Float SS_N=0: Out
MOSI	In	I/O	I/O	I/O	In
GPIO0/IO2	GPIO0: In	GPIO0: I/O IO2: I/O	GPIO0: I/O IO2: I/O	GPIO0: I/O IO2: I/O	GPIO0: In
GPIO1/IO3	GPIO0: In	GPIO1: I/O IO3: I/O	GPIO1: I/O IO3: I/O	GPIO1: I/O IO3: I/O	GPIO0: In
INT_N	OD: Float	OD: OD Out PP: Out	OD: OD Float PP: Out	OD: OD Float PP: Out	OD: Float
RST_N	In	In	In	In	In
SPIM_SCLK	In	I/O	I/O	I/O	In
SPIM_SS_N	In	I/O	I/O	I/O	In
SPIM_MISO	In	I/O	I/O	I/O	In
SPIM_MOSI	In	I/O	I/O	I/O	In
SPIM_IO2	In	I/O	I/O	I/O	In
SPIM_IO3	In	I/O	I/O	I/O	In
SDCD	In	In	In	In	In
SDCLK	Out	Out	Out	Out	Out
SDCMD	Out	I/O	I/O	I/O	Out
SDWP	In	In	In	In	In
SDD0	In	I/O	I/O	I/O	In
SDD1	In	I/O	I/O	I/O	In
SDD2	In	I/O	I/O	I/O	In
SDD3	In	I/O	I/O	I/O	In
CK	Out	Out	Out	Out	Out
CKB	Out	Out	Out	Out	Out

Pin Name	Pin Status at Different Power States				
	System Reset	ACTIVE	STANDBY	SLEEP	POWERDOWN
DQ0	In	I/O	I/O	In	In
DQ1	In	I/O	I/O	In	In
DQ2	In	I/O	I/O	In	In
DQ3	In	I/O	I/O	In	In
DQ4	In	I/O	I/O	In	In
DQ5	In	I/O	I/O	In	In
DQ6	In	I/O	I/O	In	In
DQ7	In	I/O	I/O	In	In
DQ8	In	I/O	I/O	In	In
DQ9	In	I/O	I/O	In	In
DQ10	In	I/O	I/O	In	In
DQ11	In	I/O	I/O	In	In
DQ12	In	I/O	I/O	In	In
DQ13	In	I/O	I/O	In	In
DQ14	In	I/O	I/O	In	In
DQ15	In	I/O	I/O	In	In
DQS0	In	I/O	I/O	In	In
DQSB0	In	I/O	I/O	In	In
DQS1	In	I/O	I/O	In	In
DQSB1	In	I/O	I/O	In	In
DM0	Out	Out	Out	Out	Out
DM1	Out	Out	Out	Out	Out
ADDR0	Out	Out	Out	Out	Out
ADDR1	Out	Out	Out	Out	Out
ADDR2	Out	Out	Out	Out	Out
ADDR3	Out	Out	Out	Out	Out
ADDR4	Out	Out	Out	Out	Out
ADDR5	Out	Out	Out	Out	Out
ADDR6	Out	Out	Out	Out	Out
ADDR7	Out	Out	Out	Out	Out
ADDR8	Out	Out	Out	Out	Out
ADDR9	Out	Out	Out	Out	Out
ADDR10	Out	Out	Out	Out	Out
ADDR11	Out	Out	Out	Out	Out
ADDR12	Out	Out	Out	Out	Out
ADDR13	Out	Out	Out	Out	Out
ADDR14	Out	Out	Out	Out	Out
BA0	Out	Out	Out	Out	Out
BA1	Out	Out	Out	Out	Out
BA2	Out	Out	Out	Out	Out
RAS	Out	Out	Out	Out	Out
CAS	Out	Out	Out	Out	Out
WE	Out	Out	Out	Out	Out
CKE	Out	Out	Out	Out	Out
CS0	Out	Out	Out	Out	Out
CS1	Out	Out	Out	Out	Out
ODT0	Out	Out	Out	Out	Out
ODT1	Out	Out	Out	Out	Out
RST_N_DDR	Out	Out	Out	Out	Out
VREF0	NA	NA	NA	NA	NA
VREF1	NA	NA	NA	NA	NA
RDRVDN	NA	NA	NA	NA	NA
RDRVUP	NA	NA	NA	NA	NA
DISP	Out	Out	Out	Out	Out
BACKLIGHT	Out	Out	Out	Out	Out
LVDSTX0_CLK_N	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_CLK_P	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX1_CLK_N	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_CLK_P	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX0_DATA0_N	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA0_P	Float	CH0_EN=1: Diff Out	CH0_EN=1: Diff Out	CH0_EN=1: Diff Out	Float

Pin Name	Pin Status at Different Power States				
	System Reset	ACTIVE	STANDBY	SLEEP	POWERDOWN
		Ch0_EN=0: Float	Ch0_EN=0: Float	Ch0_EN=0: Float	
LVDSTX0_DATA1_N	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA1_P	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA2_N	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA2_P	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA3_N	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX0_DATA3_P	Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	CH0_EN=1: Diff Out Ch0_EN=0: Float	Float
LVDSTX1_DATA0_N	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA0_P	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA1_N	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA1_P	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA2_N	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA2_P	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA3_N	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSTX1_DATA3_P	Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	CH1_EN=1: Diff Out Ch1_EN=0: Float	Float
LVDSRX0_CLK_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_CLK_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_CLK_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_CLK_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA0_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA0_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA1_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA1_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA2_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA2_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA3_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_DATA3_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA0_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA0_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA1_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA1_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA2_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA2_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA3_N	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX1_DATA3_P	Diff In	Diff In	Diff In	Diff In	Diff In
LVDSRX0_RPI	NA	NA	NA	NA	NA
LVDSRX1_RPI	NA	NA	NA	NA	NA
GPIO3	In	I/O	I/O	I/O	In
GPIO4	In	I/O	I/O	I/O	In
GPIO5 / TP_SCL	In	GPIO5: I/O TP_SCL: OUT	GPIO5: I/O TP_SCL: OUT	GPIO5: I/O TP_SCL: OUT	In
GPIO6 / TP_SDA	In	GPIO6: I/O TP_SDA: I/O	GPIO6: I/O TP_SDA: I/O	GPIO6: I/O TP_SDA: I/O	In
GPIO7 / TP_INT_N	In	GPIO7: I/O TP_INT_N: I/O	GPIO7: I/O TP_INT_N: In	GPIO7: I/O TP_INT_N: In	GPIO7: In TP_INT_N: In
GPIO8 / TP_RST_N	In	GPIO8: I/O TP_RST_N: Out	GPIO8: I/O TP_RST_N: Out	GPIO8: I/O TP_RST_N: Out	In
AUDIO_L	Out	Out	Out	Out	Out
AUDIO_R	Out	Out	Out	Out	Out
I2S_BCLK	In	In	In	In	In
I2S_LRCLK	In	In	In	In	In
I2S_SDAO	Out	Out	Out	Out	Out
GPIO2	In	I/O	I/O	I/O	In
GPIO9 / TIO3	In	I/O	I/O	I/O	In
GPIO10 / TIO4	In	I/O	I/O	I/O	In

Pin Name	Pin Status at Different Power States				
	System Reset	ACTIVE	STANDBY	SLEEP	POWERDOWN
GPIO11 / TIO5	In	I/O	I/O	I/O	In
GPIO12 / TIO6	In	I/O	I/O	I/O	In
GPIO13 / TIO7	In	I/O	I/O	I/O	In
GPIO14 / TIO8	In	I/O	I/O	I/O	In
GPIO15 / TIO9	In	I/O	I/O	I/O	In

Table 19 – Pin Status at Different Power States

5 Device Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the BT820 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65 to 150	°C
Floor Life (out of Bag) at Factory Ambient (30°C	168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant) *	Hours
Ambient Temperature (Power Applied)	-40 to 105	°C
VCC33A Supply Voltage	0 to +4	V
VCCIO Supply Voltage	0 to +4	V
DC input Voltage	0 to 5.5	V

Table 20 - Absolute Maximum Ratings

* If the devices are stored out of the packaging, beyond this time limit, the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 ESD and Latch-up Specifications

Description	Specification
Human Body Model (HBM)	> ± 2KV
Machine Model (MM)	> ± 200V
Latch-Up	> ± 200mA

Table 21 - ESD and Latch-up Specification

5.3 DC Characteristics

Typical condition refers to: VCC33A=3.3V, VCCIO=3.3V, Ta=25°C, unless otherwise stated.

Symbol	Description		MIN	TYP	MAX	UNIT
VCC33A_REG	LDO Regulator Input		2.97	3.3	3.63	V
VCC33A_OSC	3.3V Analog Power Supply for OSC pad		2.97	3.3	3.63	V
VCC33A_OTP	3.3V I/O Power Supply for OTP		2.97	3.3	3.63	V
VCC33A_LVDSTX	3.3V Analog Power Supply for LVDS TX		2.97	3.3	3.63	V
VCC33A_LVDSRX	3.3V Analog Power Supply for LVDS RX		2.97	3.3	3.63	V
VCC10K	Digital core logic Power Supply		0.9	1.0	1.1	V
VCC10A_LVDSRX	1.0V Analog Power Supply for LVDS RX		0.9	1.0	1.1	V
VCC10K_DDR	1.0V Digital Power Supply for DDR PHY		0.9	1.0	1.1	V
VCC10A_PLL1, VCC10A_PLL2, VCC10A_PLL3, VCC10A_PLL4	1.0V Analog Power Supply for PLL		0.9	1.0	1.1	V
VCCIO_DDR	Digital Power Supply for DDR PHY	DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		LPDDR2	1.14	1.2	1.3	V
VCCIO_DDR_CK	Digital I/O Power Supply for DDR CK/CKB and CKE	DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		LPDDR2	1.14	1.2	1.3	V
VCCIO1, VCCIO3, VCCIO4	I/O Power Supply		1.62	1.8	1.98	V
			2.25	2.5	2.75	V
			2.97	3.3	3.63	V
VCCIO2	I/O Power Supply		2.97	3.3	3.63	V
ICC1	Operating Current			170		mA
ICC2	Standby Current			110		mA
ICC3	Sleep Current			40		mA

Symbol	Description	MIN	TYP	MAX	UNIT
ICC4	Power Down Current		15		mA

Table 22 - Operating Voltage and Current

Typical condition: VCC33A_REG=3.3V, VCCIO=3.3V, Ta=25°C, unless otherwise stated.

Symbol	Description	Min	Typ	Max	Unit
Voh	Output Voltage High	VCCIO – 0.4	-	-	V
Vol	Output Voltage Low	-	-	0.4	V
Vih	Input Voltage High	2.0	-	-	V
Vil	Input Voltage Low	-	-	0.8	V
Vth	Schmitt Hysteresis Voltage	0.26	-	0.38	V
Iin	Input Leakage Current	-10	-	10	µA
Ihiz	Tri-state output Leakage Current	-10	-	10	µA
Rpu	Pull-up Resistor	-	42.8	-	KΩ
Rpd	Pull-down Resistor	-	42.8	-	KΩ

Table 23 - Digital I/O Pin Characteristics for 3.3V VCCIO

Typical condition: VCC33A_REG=3.3V, VCCIO=2.5V, Ta=25°C, unless otherwise stated.

Symbol	Description	Min	Typ	Max	Unit
Voh	Output Voltage High	VCCIO – 0.4	-	-	V
Vol	Output Voltage Low	-	-	0.4	V
Vih	Input Voltage High	1.7	-	-	V
Vil	Input Voltage Low	-	-	0.7	V
Vth	Schmitt Hysteresis Voltage	0.18	-	0.27	V
Iin	Input Leakage Current	-10	-	10	µA
Ihiz	Tri-state output Leakage Current	-10	-	10	µA
Rpu	Pull-up Resistor	-	56.4	-	KΩ
Rpd	Pull-down Resistor	-	56.4	-	KΩ

Table 24 - Digital I/O Pin Characteristics for 2.5V VCCIO

Typical condition: VCC33A_REG=3.3V, VCCIO=1.8V, Ta=25°C, unless otherwise stated.

Symbol	Description	Min	Typ	Max	Unit
Voh	Output Voltage High	VCCIO – 0.4	-	-	V
Vol	Output Voltage Low	-	-	0.4	V
Vih	Input Voltage High	1.2	-	-	V
Vil	Input Voltage Low	-	-	0.6	V
Vth	Schmitt Hysteresis Voltage	0.17	-	0.26	V
Iin	Input Leakage Current	-10	-	10	µA
Ihiz	Tri-state output Leakage Current	-10	-	10	µA
Rpu	Pull-up Resistor	-	88.6	-	KΩ
Rpd	Pull-down Resistor	-	88.6	-	KΩ

Table 25 - Digital I/O Pin Characteristics for 1.8V VCCIO

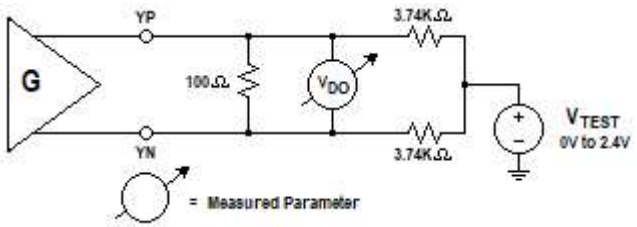


Figure 29 – Differential Output Voltage Test Circuit

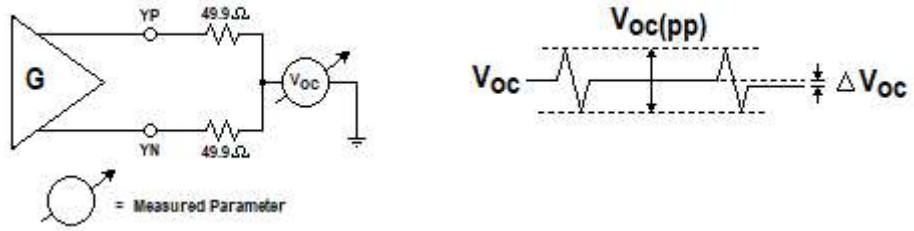


Figure 30 - Definition of Common-mode Output Voltage

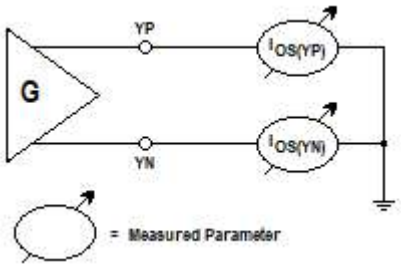


Figure 31 – Short-Circuit Measurement to Ground

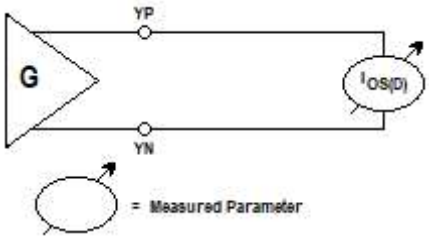


Figure 32 – Short-Circuit Measurements

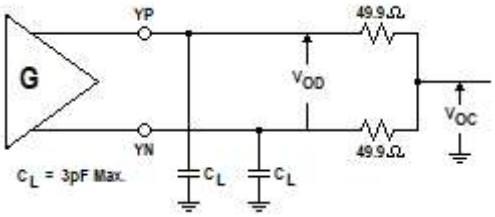


Figure 33 – Output Test Load

Symbol	Description	Conditions	Min	Typ	Max	Unit
$\|V_{OD}\|$	Differential Output Voltage	Please refer to Figure 29	247	-	454	mV
$\Delta\|V_{OD}\|$	Change of $\|V_{OD}\|$ between complementary output states		-50	-	50	mV
V_{OC}	Common-Mode Voltage	Please refer to Figure 30	1.125	1.25	1.375	V
$\Delta\|V_{OC}\|$	Change of V_{OC} between complementary output states		-50	-	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		-	50	150	mV
$\|I_{OS(YP)}\|$ $\|I_{OS(YN)}\|$	output short-circuit current	Please refer to Figure 31	-	-	24	mA
$\|I_{OS(D)}\|$	Differential short-circuit output current	Please refer to Figure 32	-	-	12	mA
C_L	Output driver capacitance load	Please refer to Figure 33	-	-	3	pF
t_{JIT}	Peak-to-peak jitter	Ideal 2^7 – 1 PRBS input at 700 Mbps	-	-	0.2	UI

Table 26 - LVDSTX Output Electrical Specification

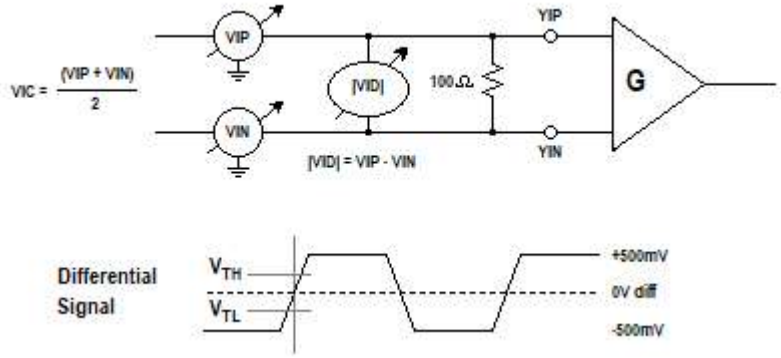


Figure 34 – Input Signal Characteristics of Receiver

Symbol	Description	Min	Typ	Max	Unit
V_{TH}	Differential input high threshold	-	-	100	mV
V_{TL}	Differential input low threshold	-100	-	-	mV
$\|V_{ID}\|$	Differential input voltage	100	-	500	mV
V_{IC}	Common-mode voltage	0.3	1.2	1.6	V

Table 27 - LVDSRX Input Electrical Specification

Symbol	Description		Min	Typ	Max	Unit
V_{IH}	Input Logic High	DDR3	VREF + 0.15	-	VCCIO_DDR + 0.4	V
		DDR3L	VREF + 0.135	-	VCCIO_DDR + 0.4	V
		LPDDR2	VREF + 0.22	-	VCCIO_DDR + 0.4	V
V_{IL}	Input Logic Low	DDR3	-0.4	-	VREF – 0.15	V
		DDR3L	-0.4	-	VREF – 0.135	V
		LPDDR2	-0.4	-	VREF – 0.22	V

Table 28 - DDR Electrical Specification

5.4 AC Characteristics

5.4.1 Input Clock

Symbol	Description	MIN	TYP	MAX	UNIT
Crystal					
F_{XTAL}	Frequency	-50ppm	38.4	50ppm	MHz
F_{DC}	Duty cycle out of crystal	45	50	55	%
C1/C2	Capacitance of C1 / C2	12	-	27	pF
External Clock					
$V_{CLK(X2)}$	Input voltage to X2 pin	3	3.3	3.63	V
t_{CLK_JIT}	External clock jitter	-	-	500	ps
t_{CLK_DC}	External clock Duty cycle	45	50	55	%

Table 29 – Input Clock Characteristics

5.4.2 QSPI Host Interface I/O Timing

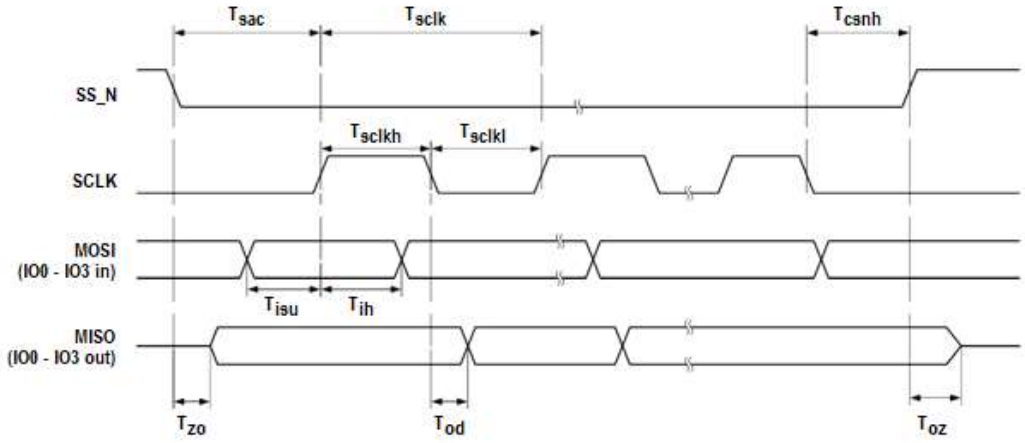


Figure 35 – Quad Host interface I/O Timing Diagram

Parameter	Description	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{sclk}	SPI clock period	16.6	-	16.6	-	16.6	-	ns
T_{sclkl}	SPI clock low duration	6.6	-	6.6	-	6.6	-	ns
T_{sclkh}	SPI clock high duration	6.6	-	6.6	-	6.6	-	ns
T_{sac}	SPI access time	3.1	-	2.9	-	2.8	-	ns
T_{isu}	SPI data input setup time	1.9	-	1.9	-	1.8	-	ns
T_{ih}	SPI data input hold time	0.5	-	0.5	-	0.6	-	ns
T_{zo}	Output enable delay	-	10.2	-	7.9	-	7.1	ns
T_{oz}	Output disable delay	-	8.6	-	6.9	-	6.4	ns
T_{od}	Output data delay	-	9.3	-	6.8	-	5.8	ns
T_{csnh}	CSN hold time	0	-	0	-	0	-	ns

Table 30 – Quad Host Interface I/O Timing

5.4.3 QSPI Flash Interface I/O Timing

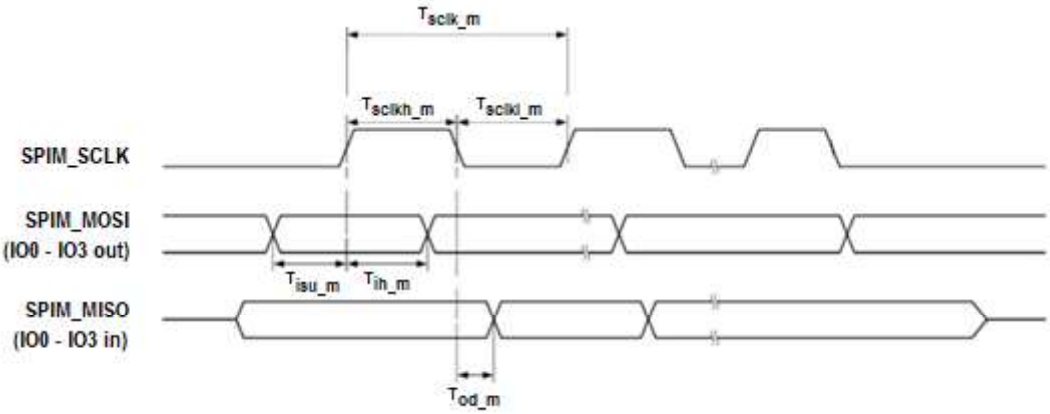


Figure 36 - SPIM I/O Timing Diagram

Parameter	Description	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{sclk_m}	SPI clock period	13.89	-	13.89	-	13.89	-	ns
T_{sclkl_m}	SPI clock low duration	6	-	6	-	6	-	ns
T_{sclkh_m}	SPI clock high duration	6	-	6	-	6	-	ns
T_{isu_m}	SPI data input setup time	1.967	-	1.795	-	1.778	-	ns
T_{ih_m}	SPI data input hold time	1.175	-	1.016	-	0.911	-	ns
T_{od_m}	Output data delay	-	3.805	-	3.378	-	3.191	ns

Table 31 - SPIM I/O Timing

5.4.4 LVDSTX Timing

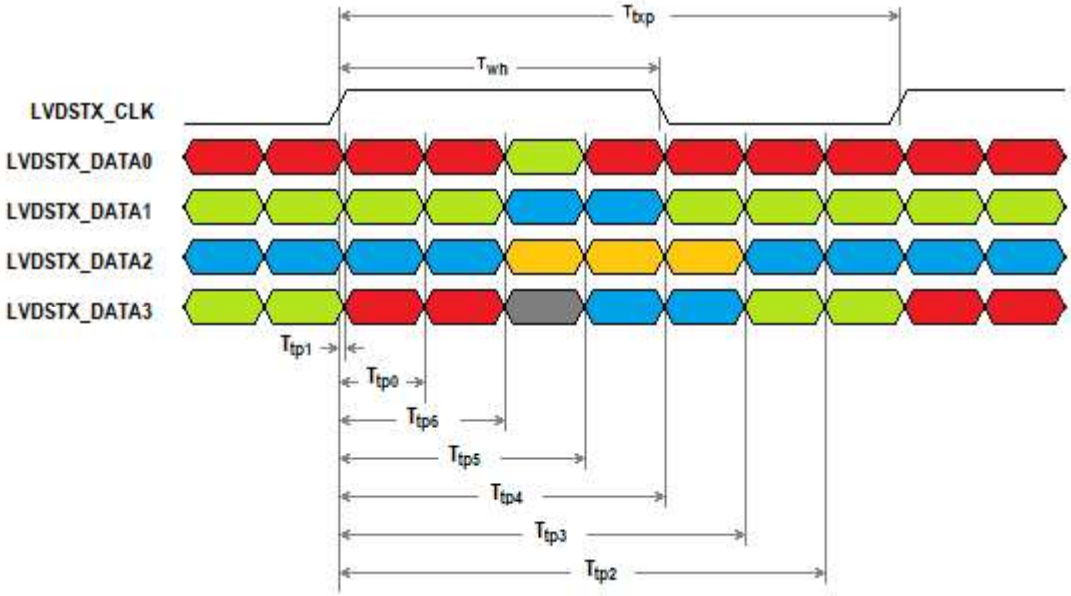


Figure 37 – LVDSTX Timing Relationship

Symbol	Description		MIN	TYP	MAX	UNIT
T_{txp}	Input clock period		12	-	28.04	ns
T_{wh}	High-level clock pulse width duration		$0.4T_{PCLK}$	-	$0.6T_{PCLK}$	ns
T_{skp}	Transmitter skew margin	Channel 0	-0.09	-	0.04	ps
		Channel 1	-0.15	-	0.02	ps
T_{tp1}	Output data position 0		$-T_{skp}$	0	T_{skp}	ps
T_{tp0}	Output data position 1		$(T_{txp}/7) - T_{skp}$	$(T_{txp}/7)$	$(T_{txp}/7) + T_{skp}$	ps
T_{tp6}	Output data position 2		$2(T_{txp}/7) - T_{skp}$	$2(T_{txp}/7)$	$2(T_{txp}/7) + T_{skp}$	ps
T_{tp5}	Output data position 3		$3(T_{txp}/7) - T_{skp}$	$3(T_{txp}/7)$	$3(T_{txp}/7) + T_{skp}$	ps
T_{tp4}	Output data position 4		$4(T_{txp}/7) - T_{skp}$	$4(T_{txp}/7)$	$4(T_{txp}/7) + T_{skp}$	ps

T_{tp3}	Output data position 5	$5(T_{txp}/7) - T_{skp}$	$5(T_{txp}/7)$	$5(T_{txp}/7) + T_{skp}$	ps
T_{tp2}	Output data position 6	$6(T_{txp}/7) - T_{skp}$	$6(T_{txp}/7)$	$6(T_{txp}/7) + T_{skp}$	ps

Table 32 – LVDSTX Timing Relationship

5.4.5 LVDSRX Timing

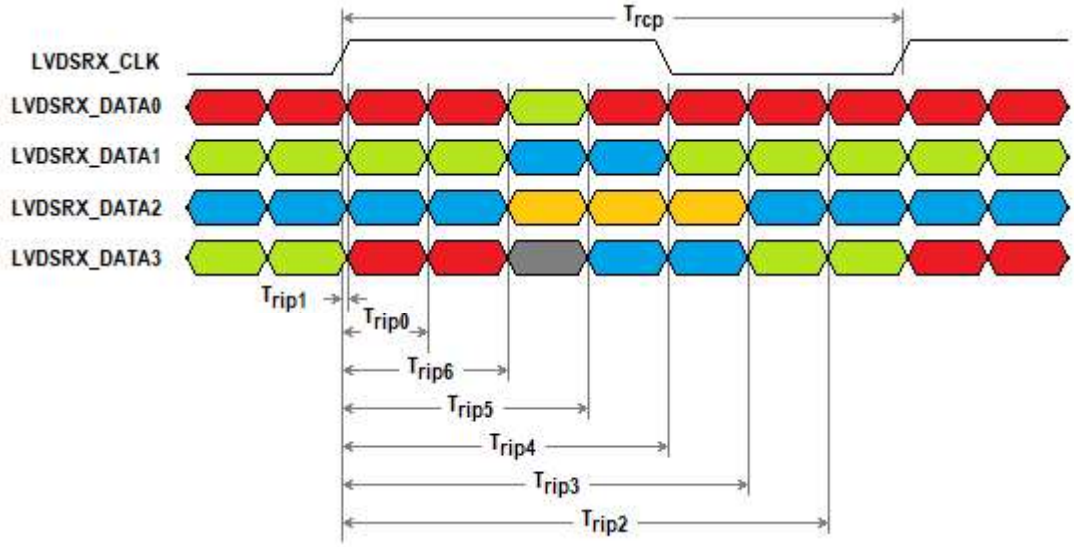


Figure 38 - LVDSRX Timing Relationship

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{rcp}	Input clock period	-	7	-	100	ns
T_{sk}	Receiver skew margin	RCLK < 85 MHz	-400	0	400	ps
		RCLK = 135 MHz	-170	-	170	ps
		RCLK = 142 MHz	-110	-	110	ps
T_{rip1}	Input data position 0	-	$-T_{sk}$	0	T_{sk}	ps
T_{rip0}	Input data position 1	-	$(T_{rcp}/7) - T_{sk}$	$T_{rcp}/7$	$(T_{rcp}/7) + T_{sk}$	ps
T_{rip6}	Input data position 2	-	$2(T_{rcp}/7) - T_{sk}$	$2(T_{rcp}/7)$	$2(T_{rcp}/7) + T_{sk}$	ps
T_{rip5}	Input data position 3	-	$3(T_{rcp}/7) - T_{sk}$	$3(T_{rcp}/7)$	$3(T_{rcp}/7) + T_{sk}$	ps
T_{rip4}	Input data position 4	-	$4(T_{rcp}/7) - T_{sk}$	$4(T_{rcp}/7)$	$4(T_{rcp}/7) + T_{sk}$	ps
T_{rip3}	Input data position 5	-	$5(T_{rcp}/7) - T_{sk}$	$5(T_{rcp}/7)$	$5(T_{rcp}/7) + T_{sk}$	ps
T_{rip2}	Input data position 6	-	$6(T_{rcp}/7) - T_{sk}$	$6(T_{rcp}/7)$	$6(T_{rcp}/7) + T_{sk}$	ps
T_{dll}	DLL locking time	-	-	-	100	µs
T_{dll_reset}	DLL reset time	-	10	-	-	µs

Table 33 – LVDSRX Timing Relationship

5.4.6 Audio Output Timing

5.4.6.1 Stereo Audio

Parameter	Description	MIN	TYP	MAX	UNIT
$T_{C(DELTA-SIGMA)}$	Delta-Sigma Carrier Frequency	-	27.7	-	ns
$T_{C(PWM)}$	PWM Carrier Frequency	-	7.14	-	µs

Table 34 – Stereo Audio Output Ports Carrier frequency

5.4.6.2 I2S Interface

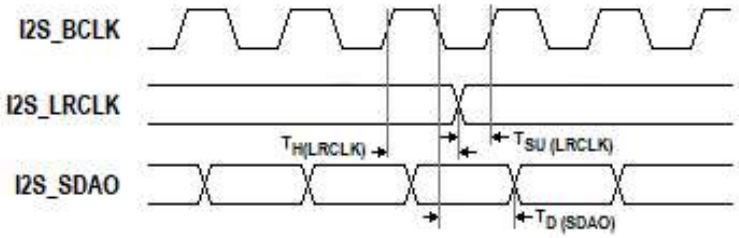


Figure 39 – I2S Slave I/O Timing

Parameter	Description	MIN	TYP	MAX	UNIT
$T_{SU(LRCLK)}$	I2S_LRCLK Setup time	6	-	-	ns
$T_{H(LRCLK)}$	I2S_LRCLK_hold time	10	-	-	ns
$T_{D(SDAO)}$	I2S_LRCLK delay time	0	-	11	ns

Table 35 – I2S Slave I/O Timing

6 Application Information

6.1 Input Clock

6.1.1 Crystal Source

The BT820 supports the use of an external crystal oscillator operating at 38.4MHz as a clock source as described in section **Error! Reference source not found.**. The load capacitance is necessary to ensure the proper operation of the crystal within the expected parameters. The load capacitance refers to the amount of capacitance seen between the terminals of the crystal in the circuit. The discrete capacitors, C1 and C2 are used to provide the correct load capacitance.

The discrete capacitors, C1 and C2 can be calculated using Equation 1.

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_{STRAY}$$

Equation 1

Where:

C_L is the total load capacitance seen by the crystal circuit.
C_{STRAY} is the stray capacitance on the PCB
C1 and C2 are the discrete load capacitors. These capacitors must be selected to make C_L close to the load capacitance specified by the crystal manufacturer

6.1.2 PCB Design Guidelines for Crystal Oscillator

1. Place the crystal close to X1/CLK and X2 ball pads.
2. Place the C1 and C2 load capacitors close to the crystal pins.
3. Place any noisy components or power supplies away from the crystal and it load capacitors.
4. Keep the traces connecting the crystal, capacitors, and X1/CLK and X2 ball pads as short and as wide as possible.
5. Avoid routing any high-frequency signals near the crystal oscillator circuit.
6. Avoid routing any signals under the crystal oscillator circuit.
7. Avoid right angle bends on these traces
8. Keep the area under the crystal well-grounded

To minimize on-board noise caused by the supply voltage and ground, BT820 provides dedicated VCC33A_OSC and GND_OSC. The chip decoupling capacitors can be placed close to VCC33A_OSC and GNDA_OSC as shown in Figure 40.

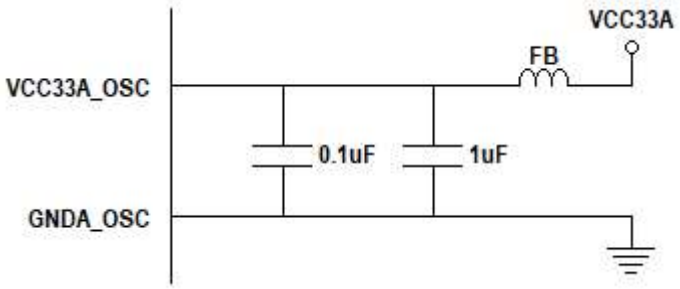


Figure 40 - Typical VCC33A_OSC Application Circuit

6.1.3 Phase Locked Loop

There are 4 phase Locked Loops (PLLs) inside the chip. BT820 provides dedicated VCC10A_PLL and GNDA_PLL for each PLL. To minimize on-board noise caused by the supply voltage and ground, the chip decoupling capacitors can be placed close to each VCC10A_PLL and GNDA_PLL as shown in Figure 41.

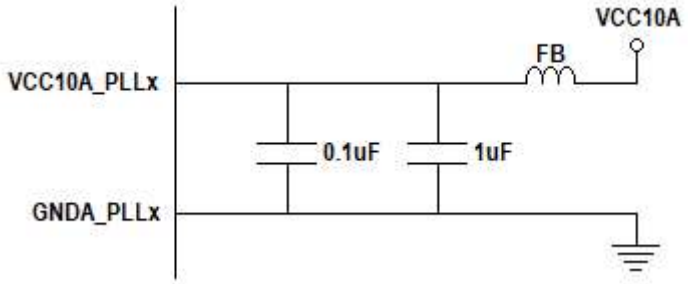


Figure 41 - Typical VCC10A_PLL Application Circuit

6.2 Video Input / Outputs

BT820 supports 2 LVDS transmit channels of 4 data lanes per channels and 2 LVDS receive channels of 4 data lanes per channels.

6.2.1 PCB Design Guidelines for LVDS channels

The PCB design guidelines for LVDS transmit channels and LVDS receives channels are the similar.

1. 100Ω±10% impedance is recommended for all differential traces
2. The data pair length mismatch should be less than ±5mils.
3. Data signal traces must match in length, number of Vias and on the same layer
4. Data signal trace length must match the clock signals
5. It is recommended that the Data signals be referenced to a single solid GND plane
6. Traces must not cross different planes

6.3 DDR Interface

The DDR interface supports DDR3/DDR3L/LPDDR2 DRAM with data rates of 800MT/s to 1333MT/s and data bit width of 16bits only. The interface supports DRAM size of 8Gbits, 4Gbits, 2Gbits, 1Gbits, 512Mbits. Support for 8Gbits DRAM is limited to the use of 2 ranks of 4Gbits DRAM.

6.3.1 PCB Design Guidelines for DDR3/DDR3L

Parameter	Design Guideline
Trace characteristics	• 50Ω±10% impedance is recommended for all single-ended traces • 85Ω±10% impedance is recommended for all differential traces • Unused Via pads on the traces must be removed. • Apply 45° bending routing instead of 90° bending routing for all signals
Power/Ground domain (VCCIO_DDR, VCC10K_DDR, GND)	• Power / GND (Reference plane) must be routed as a solid plane. • Power plane must have a solid GND plane
Clock (CK, CKB)	• CK, CKB are differential pair signals • CK and CKB length mismatch should be less than ±5 mils • It is recommended that the clock signals to maintain 3W spacing from other signals. • It is recommended that the clock signals be reference to a single solid GND plane • Traces must not cross different planes

Data Strobe (DQS0, DQSB0, DQS1, DQSB1)	• DQS0, DQSB0 are differential pair signals for lower DQ Byte Lane • DQS1, DQSB1 are differential pair signals for upper DQ Byte Lane • DQS and DQSB length mismatch should be less than ±5 mils • It is recommended that the DQS signals to maintain 3W spacing from other signals. • It is recommended that the DQS signals be referenced to a single solid GND plane. • DQS and DQSB length must match the clock signals. • Traces must not cross different planes
Data (DQ, DM)	• Data signal traces must match in length, number of Vias and on the same layer • Data signal trace length must match the clock signals • A maximum of two Vias is recommended • It is recommended that the Data signals be referenced to a single solid GND plane • Traces must not cross different planes
Address/Command (ADDR, BA0, BA1, BA2, CAS, RAS, WE)	• Address/Command signal traces must match in length, number of Vias and on the same layer • Address/Command signal trace length must match the clock signals. • A maximum of two Vias is recommended • The Address/Command signals can be referenced to a single solid power plane or a single solid GND plane • Traces must not cross different planes

Control
(CKE, CS0, CS1, ODT0,
ODT1, RST_N_DDR)
	• Control signal traces must match in length, number of Vias and on the same layer.
	• Control signal traces length must match the clock signals.
	• A maximum of two Vias is recommended.
	• Enough edge-to-edge trace separation to reduce crosstalk.
	• Traces must not cross different planes
	• When using 2 ranks of DRAM:
	  ○ Connect CS0 to CS of the first DRAM
	  ○ Connect ODT0 to ODT of the first DRAM.
	  ○ Connect CS1 to CS of the second DRAM
	• Connect ODT1 to ODT of the second DRAM

Reference (Vref0, Vref1)	• Connect a voltage that is half the voltage of VCCIO_DDR using a voltage regulator or a voltage divider.

Table 36: PCB Design Guidelines for DDR3/DDR3L

6.3.2 PCB Design Guidelines for LPDDR2

Parameter	Design Guideline
Trace characteristics	• 50Ω±10% impedance is recommended for all single-ended traces • 85Ω±10% impedance is recommended for all differential traces • Unused Via pads on the traces must be removed. • Apply 45° bending routing instead of 90° bending routing for all signals
Power/Ground domain (VCCIO_DDR, VCC10K_DDR, GND)	• Power / GND (Reference plane) must be routed as a solid plane. • Power plane must have a solid GND plane
Clock (CK, CKB)	• CK, CKB are differential pair signals • CK and CKB length mismatch should be less than ±5 mils • It is recommended that the clock signals to maintain 3W spacing from other signals. • It is recommended that the clock signals be referenced to a single solid GND plane • Traces must not cross different planes
Data Strobe (DQS0, DQSB0, DQS1, DQSB1)	• DQS0, DQSB0 are differential pair signals for lower DQ Byte Lane • DQS1, DQSB1 are differential pair signals for upper DQ Byte Lane • DQS and DQSB length mismatch should be less than ±5 mils • It is recommended that the DQS signals to maintain 3W spacing from other signals.

Parameter	Design Guideline
	• It is recommended that the DQS signals be referenced to a single solid GND plane. • DQS and DQSB length must match the clock signals. • Traces must not cross different planes
Data (DQ, DM)	• Data signal traces must match in length, number of Vias and on the same layer • Data signal trace length must match the clock signals • A maximum of two Vias is recommended • It is recommended that the Data signals be referenced to a single solid GND plane • Traces must not cross different planes
Address/Command (ADDR, BA0, BA1, BA2, CAS, RAS, WE)	• Address/Command signal traces must match in length, number of Vias and on the same layer • Address/Command signal trace length must match the clock signals. • A maximum of two Vias is recommended • The Address/Command signals can be referenced to a single solid power plane or a single solid GND plane • Traces must not cross different planes • BA0, BA1, BA2, RAS, CAS, and WE are left not connect.
Control (CKE, CS0, CS1, ODT0, ODT1, RST_N_DDR)	• Control signal traces must match in length, number of Vias and on the same layer. • Control signal traces length must match the clock signals. • A maximum of two Vias is recommended. • Enough edge-to-edge trace separation to reduce crosstalk. • Traces must not cross different planes • ODT0, ODT1, RST_N_DDR are left not connected.
Reference (Vref0, Vref1)	• Connect a voltage that is half the voltage of VCCIO_DDR using a voltage regulator or a voltage divider.

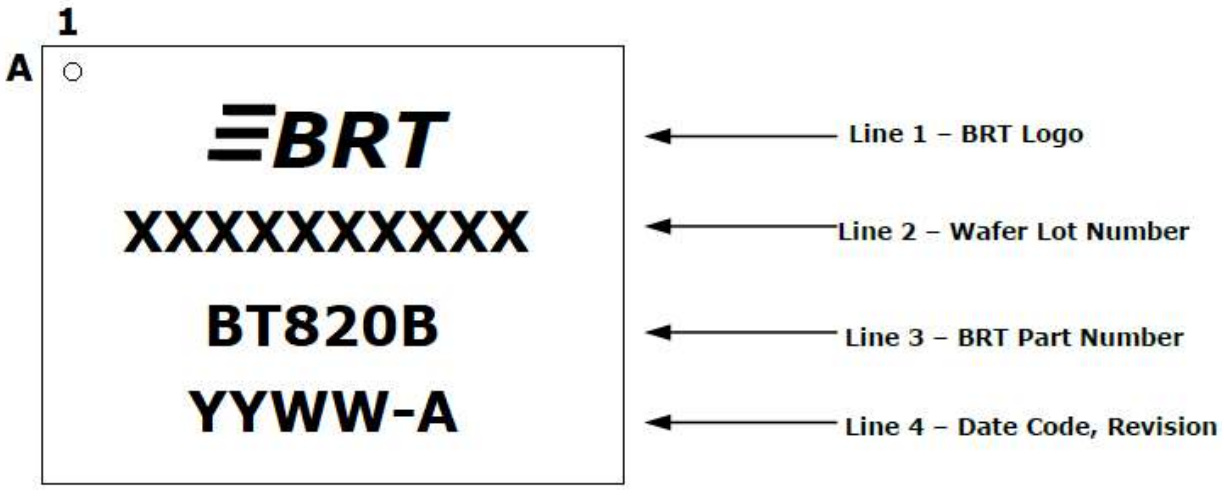
Table 37: PCB Design Guideline for LPDDR2

7 Package Parameters

The BT820 is available in 329 Balls LFBGA Package. The package dimensions, markings and solder reflow profile for the package are described in the following sections.

7.1 Part Marking

7.1.1 Top Side



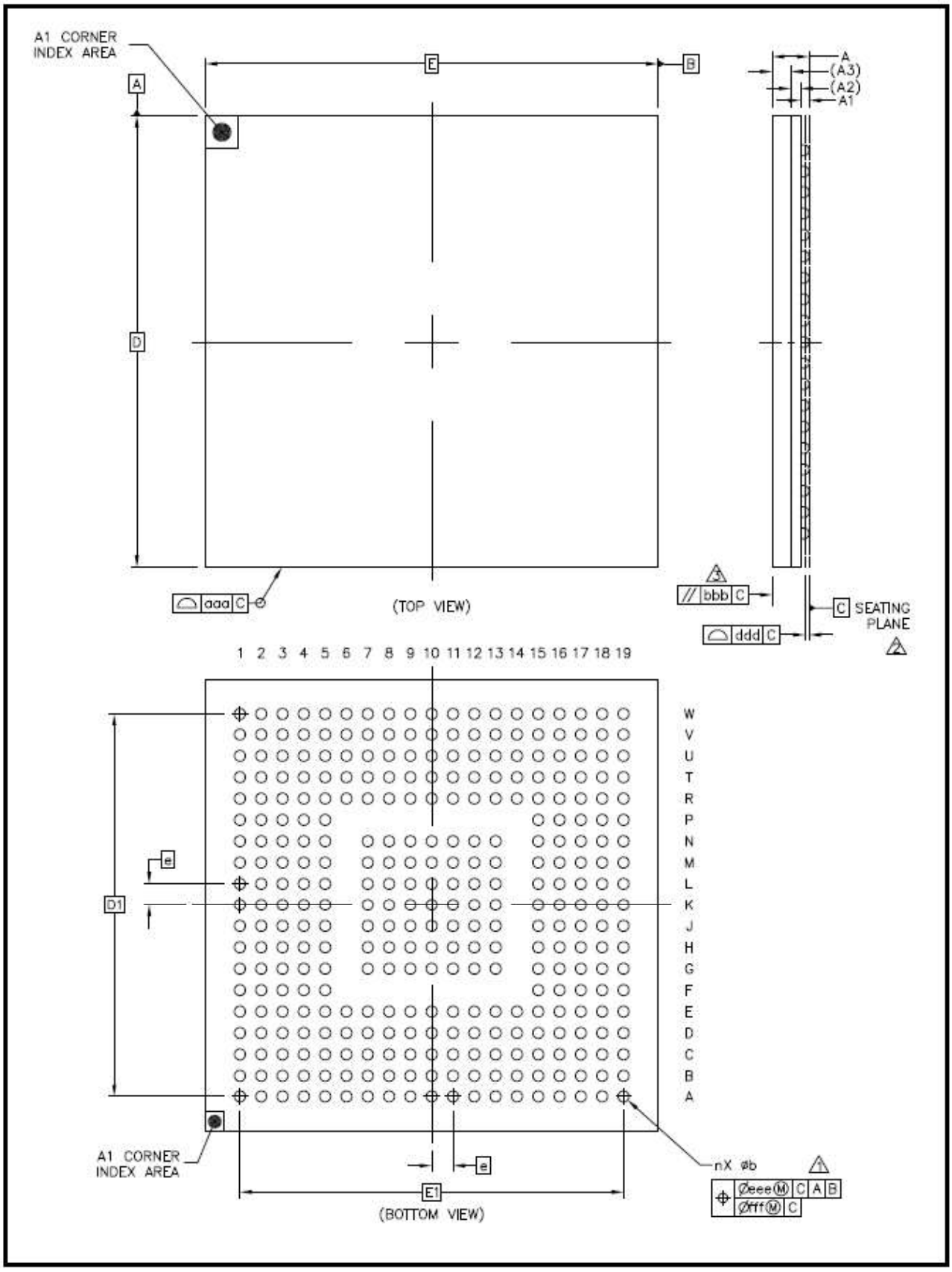
Notes:

1. YYWW = Date Code, where YY is year and WW is week number.

7.1.2 Bottom Side

No markings should be placed on the bottom side.

7.2 329 BALLS LFBGA Package Dimensions



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.5
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.36	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		17	BSC
	E		17	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.36	---	0.46
BALL PITCH	e		0.8	BSC
BALL COUNT	n		329	
EDGE BALL CENTER TO CENTER	D1		14.4	BSC
	E1		14.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 42 – 329 Ball LFBGA Package Dimensions

Note:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plan C.
2. Datum C (seating plane) is defined by the spherical crowns of the solder balls
3. Parallelism measurement shall exclude any effect of mark on top surface of package

8 Contact Information

Refer to https://brtchip.com/contact-us/ for contact information.

Distributor and Sales Representatives

Please visit the Distribution Network – IC & Module (brtchip.com) page for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

BRTAN_086 BT82X Series Programming Guide

Acronyms and Abbreviations

Terms	Description
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
EVE	Embedded Video Engine
GPS	Global Positioning System
HMI	Human Machine Interfaces
HSYNC	Horizontal Synchronization
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound Bus
IMA-ADPCM	Interactive Multimedia Association - Adaptive Differential Pulse Code Modulation
JPEG	Joint Photographic Experts Group
JEIDA	Japanese Electronic Industry Development Association
LCD	Liquid-Crystal Display
LVDS	Low-Voltage Differential Signalling
LPDDR	Low-Power Double Data Rate
MCU	Microcontroller Unit
OTP	One-Time Programmable
PCM	Pulse Code Modulation
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
QSPI	Qual Serial Peripheral Interface
RGB	Red, Green Blue
ROM	Read Only Memory
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
SPI	Serial Peripheral Interface
VESA	Video Electronics Standards Association
VSYNC	Vertical Synchronization

Appendix B – List of Figures and Tables

List of Figures

List of Tables

Appendix C – Revision History

Document Title: BT820 Framebuffer based Embedded Video Engine Datasheet
Document Reference No.: BRT_000427
Clearance No.: BRT#214
Product Page: https://brtchip.com/product-category/products/
Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	03-10-2024