



BRT_TN_005

BT81x Errata Technical Note

Version 1.0

Issue Date: 10-03-2024

The intention of this errata technical note is to document a detailed description of known functional or electrical issues with the BRTChip's BT81x series devices, including BT815, BT816, BT817, BT818, BT817A.

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1 BT81x Revision – Part Numbers

BT81x part numbers are listed in the following table. The suffix letter following the date code on the package marking identifies the device revision.

Note: BT817Q/BT818Q/BT817AQ RevA is an internal revision, never released to market.

Part Number and Revision	Description
BT815Q RevA	EVE3 with capacitive touch
BT816Q RevA	EVE3 with resistive touch
BT817Q RevB	EVE4 with capacitive touch
BT818Q RevB	EVE4 with resistive touch
BT817AQ RevB	EVE4 with capacitive touch, automotive graded

Table 1 - BT81x Part Numbers

2 Errata History Table – Functional Issues

Functional Errata	Short Description	Errata occurs in device revision
BT815Q/BT816Q	Display list instruction over fetch	Rev A
BT817Q/BT818Q/BT817AQ	Display list instruction over fetch	Rev B

Table 2 – Functional Issues

2.1 Errata History Table – Electrical and Timing Specification Deviations

Deviations	Short Description	Errata occurs in device revision
-	No known issues	-

Table 3 – Electrical and Timing Specification Deviations

3 Functional Issues of BT81x

3.1 Display list instruction overfetch

Introduction:

In the graphics engine, display list fetch is double-operation: the hardware fetches and decodes two 32-bit instructions per clock. When the **DISPLAY** instruction, which marks the end of display list, is placed in an even slot, the following instruction in the odd slot is erroneously fetched and can be partially executed by some bitmap pipeline stages. The table below shows the layout of **RAM_DL** content when the issue happens:

Instruction 1	Instruction 0
Instruction 3	Instruction 2
...	...
Instruction 2N+1	Instruction 2N (DISPLAY)

The specific problematic instruction is **BITMAP_SIZE**. If it occurs after the **DISPLAY** instruction, it is executed by the graphics engine, and erroneously sets the height parameter of current bitmap handle. Consequently, the rendered image associated with the impacted bitmap handle could be enlarged or shortened vertically.

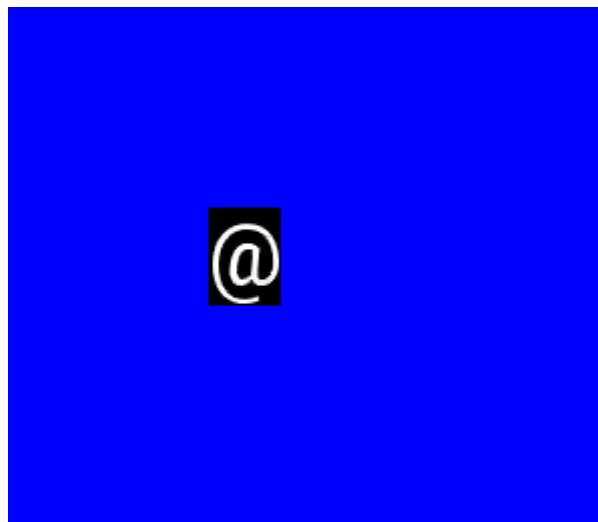
Note that the problematic extra instruction **BITMAP_SIZE** could be either left over by an older display list using the same **RAM_DL**, or by chance the initial content of the **RAM** upon chip power on if that **RAM_DL** location is not used in any older display list.

For example, given the following display list:

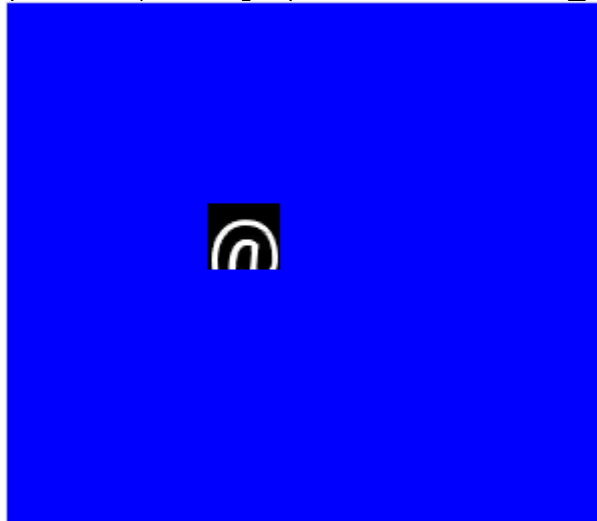
```

CLEAR_COLOR_RGB(0, 0, 254) // Instruction 0
CLEAR(1, 1, 1) // Instruction 1
BITMAP_HANDLE(31) // Instruction 2
BEGIN(BITMAPS) // Instruction 3
BLEND_FUNC(SRC_ALPHA, ZERO) // Instruction 4
VERTEX2II(100, 100, 31, '@') // Instruction 5
DISPLAY() // Instruction 6
BITMAP_SIZE(NEAREST, BORDER, BORDER, 36, 33) // Instruction 7
  
```

The expected image is:



Since instruction 7 is partially executed, the height parameter of **BITMAP_SIZE** is set to 33:



Exception:

When the erroneously fetched instruction is not **BITMAP_SIZE**, there's no impact to the display content. When the **DISPLAY** instruction is placed in the odd slot, there's no impact to the display content.

Workaround:

The software workarounds are as follows:

Identify the end of display list and append it with an *additional* **DISPLAY** instruction, guaranteeing that the erroneous fetch (if any) does nothing. For example:

```

CLEAR_COLOR_RGB(0, 0, 254)           // Instruction 0
CLEAR(1, 1, 1)                       // Instruction 1
BITMAP_HANDLE(31)                    // Instruction 2
BEGIN(BITMAPS)                       // Instruction 3
BLEND_FUNC(SRC_ALPHA, ZERO)         // Instruction 4
VERTEX2II(100, 100, 31, '@')        // Instruction 5
DISPLAY()                             // Instruction 6
DISPLAY()                             // Instruction 7
  
```

At instruction 7, an additional **DISPLAY** instruction is added, which prevents the unexpected impact of erroneously fetched instruction.

However, when the following coprocessor commands are used, the workaround above is not applicable because these commands generate the **DISPLAY** instruction and swap the display list immediately:

- *CMD_CALIBRATE*
- *CMD_SPINNER*
- *CMD_LOGO*
- *CMD_RUNANIM*
- *CMD_TESTCARD*
- *CMD_CLEARCACHE*

In this scenario, the workaround is to reset **RAM_DL** to zero before initiating the display list, effectively populating **RAM_DL** with **DISPLAY** instructions. For example:

```
CMD_DLSTART ()  
CMD_MEMZERO (RAM_DL, 8192)  
CLEAR (1, 1, 1)  
CMD_TEXT (80, 30, 27, OPT_CENTER, "PLEASE TAP ON THE DOT")  
CMD_CALIBRATE ()
```

Coprocessor command **CMD_MEMZERO** is added to reset the **RAM_DL** to zero, which guarantees the display list is ended with at least two **DISPLAY** instructions.

4 Electrical and Timing Specification deviations of BT81x

There are no known electrical or timing problems with any revision of silicon.

5 Contact Information

Refer to <https://brtchip.com/contact-us/> for contact information.

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Appendix A – References

Document References

NA

Acronyms and Abbreviations

Terms	Description
EVE	Embedded Video Engine

Appendix B – List of Tables & Figures

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Appendix C – Revision History

Document Title: BRT_TN_005 BT81x Errata
Document Reference No.: BRT_000432
Clearance No.: BRT#208
Product Page: <https://brtchip.com/product-category/products/>
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Revision	Changes	Date
1.0	Initial Release	10-03-2024