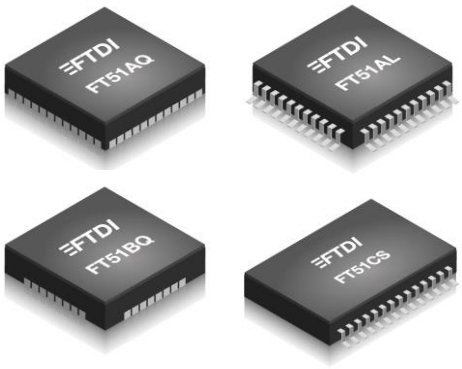
Future Technology Devices International Ltd.

FT51A

(Advanced Microcontroller with 8051 Compatible Core)



The FT51A is a multi-featured device that can be targeted at a wide range of functions or applications:

- Industry compatible 8051 core running at a maximum frequency of 48MHz.
- 8 KB of data memory
- 16 KB of multi-time programmable (MTP) memory
- 16 KB of shadow memory for fast read access by the core.
- USB 2.0 Full Speed hub controller allowing cascading of multiple FT51A devices
- USB 2.0 Full Speed device controller compatible to FT12 series
- Supports up to 8 bi-directional endpoints with 2 x 1 KB USB endpoint buffers
- Max packet size is 504 bytes for USB isochronous endpoint and 64 bytes for control / bulk / interrupt endpoint
- Double buffer scheme for any endpoint, increases data transfer throughput
- Fully integrated clock generation with no external crystal required
- Data transfer rates from 300 baud to 3M baud (RS422, RS485, and RS232) at TTL levels
- PWM Controller
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity
- USB Battery Charger Detection allowing optimized charging profile
- Supports DMA operation
- I^2C Master & Slave functionality
- SPI Master & Slave functionality
- 245 FIFO module provides a simple FIFO interface to transmit and receive data
- Timer and Watchdog
- Up to 16 dedicated digital IO pins
- Up to 16 multiplexed analogue / digital IO pins
- Support ADC function on analogue IO pins
- IO Mux control for maximum flexibility in pin selection
- Configurable IO pin output drive strength; 4 mA (min) and 16 mA (max)
- +5V Single Supply Operation
- Internal 3.3V/1.8V voltage regulators
- Integrated power-on-reset circuit
- Low operating and suspend current; 20 mA (active) and 150 uA (suspend)
- Extended operating temperature range; -40 to 85°C
- Available in compact Pb-free, RoHS compliant packages:
  - 48-pin WQFN
  - 44-pin LQFP
  - 32-pin WQFN
  - 28-pin SSOP

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1 Typical Applications

- USB Data Acquisition
- General Purpose Microcontroller
- Sensor and Monitoring control
- Mass storage data transfers across all segments, including medical, industrial data-logger, power-metering, and test instrumentation
- USB to RS232/RS422/RS485 Converters
- Incorporate USB interface to enable PC transfers for development systems
- Interfacing MCU/PLD/FPGA based designs to add USB connectivity
- Industrial equipment control systems
- POS systems
- USB Bar Code Readers
- Internet of things application
- Home automation control systems

1.1 Part Numbers

Part Number	Package
FT51AQ-R	48 Pin QFN, body 7x7x0.75 mm, pitch 0.5mm, Taped and Reel, 3000 per reel
FT51AQ-T	48 Pin QFN, body 7x7x0.75 mm, pitch 0.5mm, Tray packing, 490 per tray
FT51AL-R	44 Pin LQFP, body 10x10x1.4 mm, pitch 0.8mm, Taped and Reel, 1000 per reel
FT51AL-T	44 Pin LQFP, body 10x10x1.4 mm, pitch 0.8mm, Tray packing, 160 per tray
FT51BQ-R	32 Pin QFN, body 6x6x0.75 mm, pitch 0.5mm, Taped and Reel, 3000 per reel
FT51BQ-T	32 Pin QFN, body 6x6x0.75 mm, pitch 0.5mm, Tray packing, 490 per tray
FT51CS-R	28 Pin SSOP, body 10.2x5.3x1.75 mm, pitch 0.65mm, Taped and Reel, 2000 per reel
FT51CS-U	28 Pin SSOP, body 10.2x5.3x1.75 mm, pitch 0.65mm, Tube packing, 47 per tube

Table 1-1 – Part Numbers

1.2 USB Compliant

The FT51A is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001701 (Rev C).

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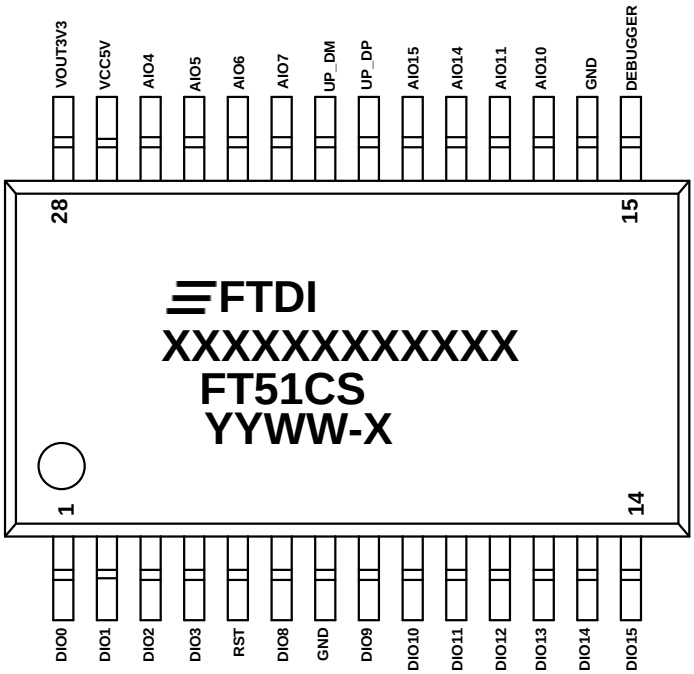
2 Device Pin Out and Signal Description

FT51A is available in 4 packages: 28 pin SSOP, 32 pin WQFN, 44 pin LQFP and 48 pin WQFN.

2.1 Pin Out - 28 pin SSOP



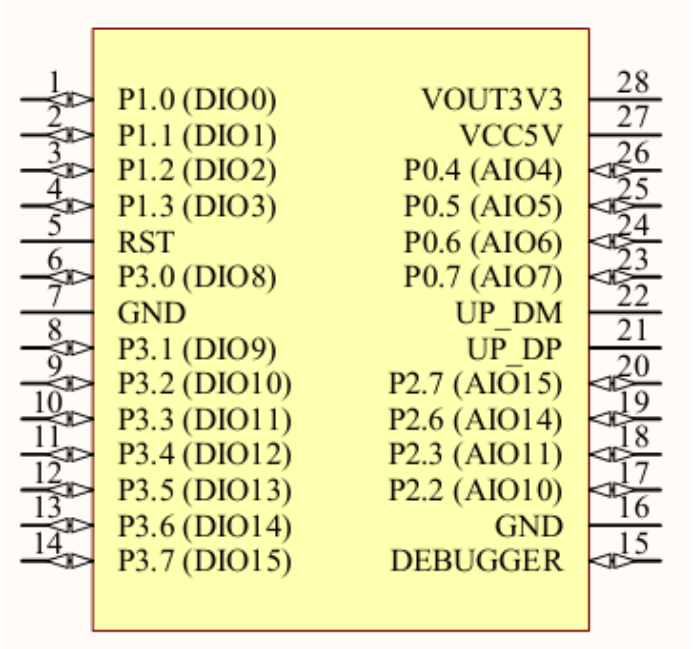


Figure 2-1 - 28 Pin SSOP Package

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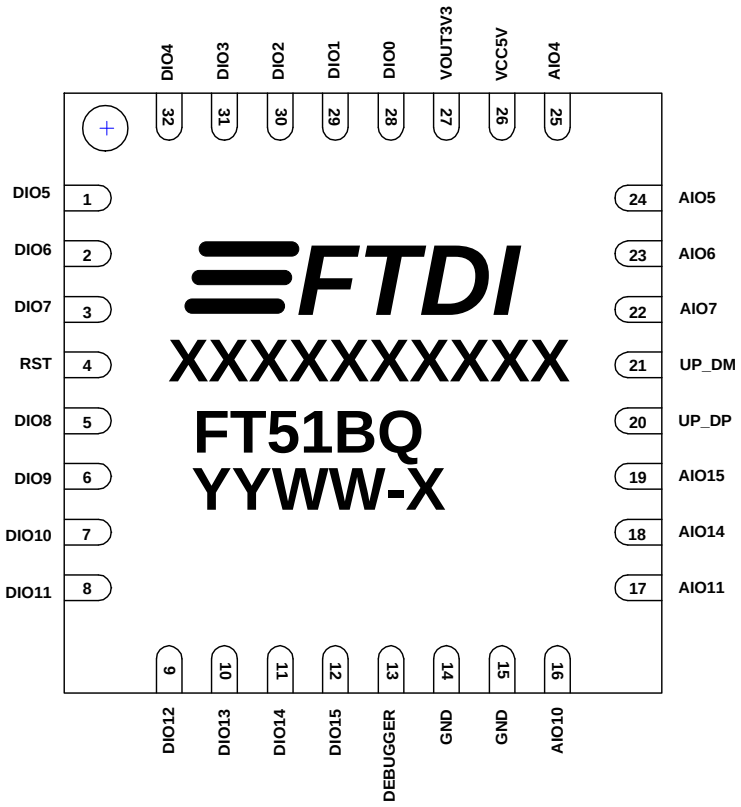
2.2 Pin Out - 32 pin WQFN



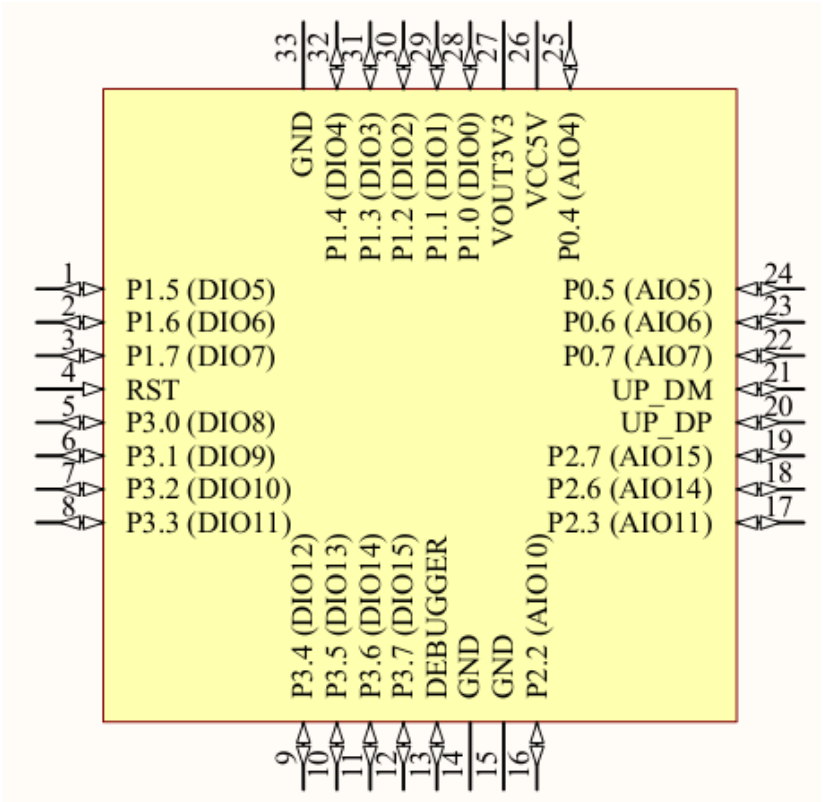


Figure 2-2 - 32 Pin WQFN Package

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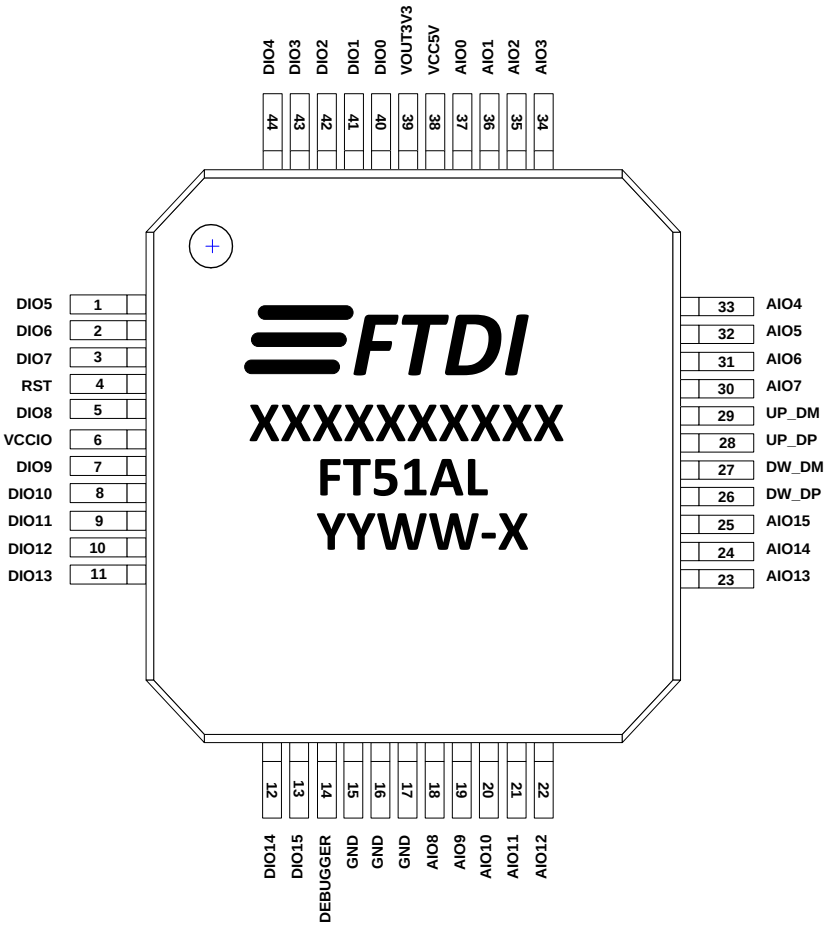
2.3 Pin Out - 44-Pin LQFP



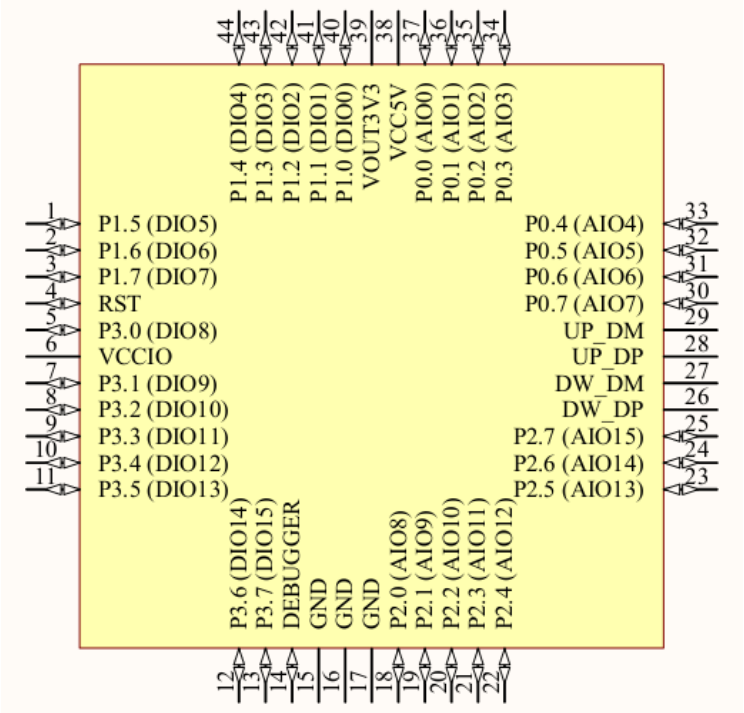


Figure 2-3 - 44 Pin LQFP Package

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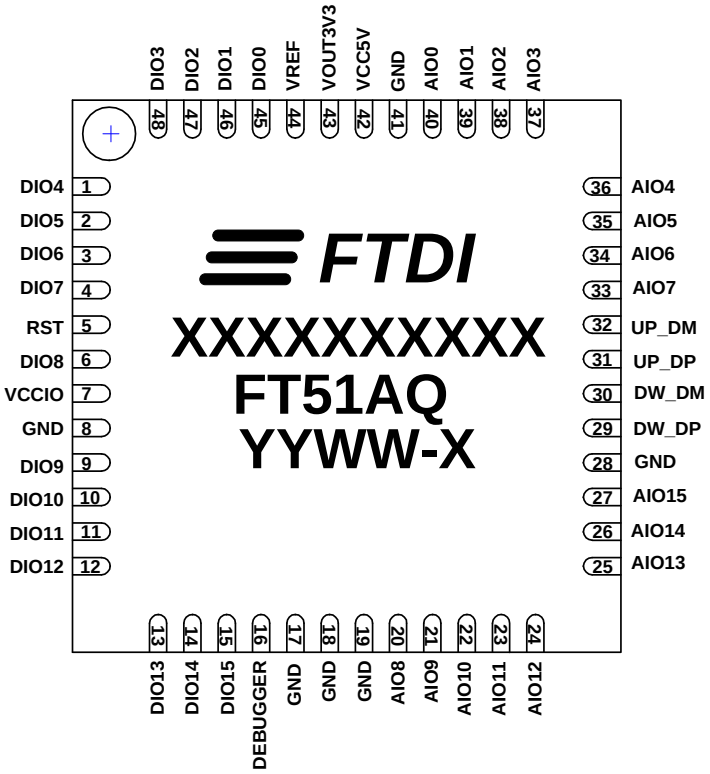
2.4 Pin Out - 48-Pin WQFN



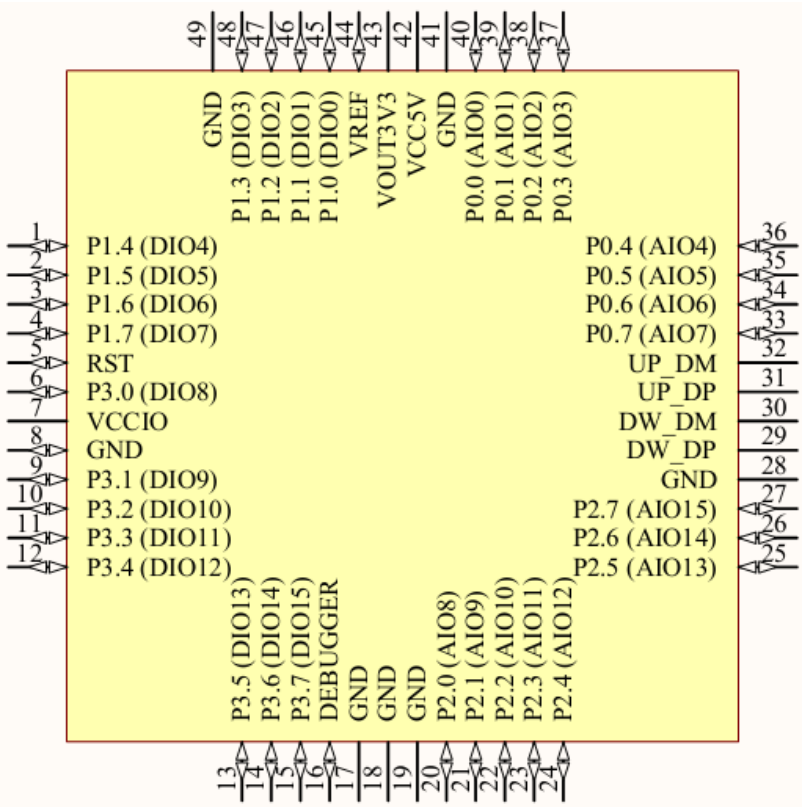


Figure 2-4 - 48 Pin WQFN Package

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2.5 Pin Configuration Description

Pin Nos.				Name	Type	Description
48 pin	44 pin	32 pin	28 pin			
42	38	26	27	** VCC5V	POWER Input	5 V (or 3.3 V) supply to IC
7	6	-	-	VCCIO	POWER Input	1.8V – 3.3V supply for the IO pins. This option is ONLY available on the 44 & 48 pin packages. A fixed 3.3V supply from the internal regulator is supplied to the IO pins for the 28 and 32 pin packages
43	39	27	28	** VOUT3V3	POWER Output	3.3V regulator output. May be used to power VCCIO pin. Note that a 100nF capacitor should be connected to VOUT3V3 for proper operation. This output can also be used to power external circuitry up to a maximum current rating of 50mA (typ).
8, 17, 18, 19, 28, 41, 49*	15,16, 17	14,15, 33*	7, 16	GND	POWER Input	Ground

Table 2-1 – Power and Ground

* Pin 49 of WQFN48 or pin 33 of WQFN32 is the exposed centre pad under the packaged IC. Connect to GND.

** If VCC5V is supplied by 3.3V then VOUT3V3 must also be driven by the same 3.3V source.

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Pin Nos.				Name	Type	Description
48 pin	44 pin	32 pin	28 pin			
30	27	-	-	DW_DM	INPUT/ OUTPUT	Downstream USB Data Signal Minus.
29	26	-	-	DW_DP	INPUT/ OUTPUT	Downstream USB Data Signal Plus.
32	29	21	22	UP_DM	INPUT/ OUTPUT	Upstream USB Data Signal Minus.
31	28	20	21	UP_DP	INPUT/ OUTPUT	Upstream USB Data Signal Plus.
5	4	4	5	RST	INPUT	Device Reset. Active HIGH
44	-	-	-	VREF	INPUT	Reference voltage. Connect to VOUT3V3.
16	14	13	15	DEBUGGER	INPUT/ OUTPUT	Chip Debug Port
1,2,3,4,6, 9,10,11,12 13,14,15 45,46,47,48	1,2,3,5,7,8 9,10,11 12,13, 40,41,42 43,44	1,2,3 5,6,7 8,9,10 11,12, 28,29,30 31,32	1,2,3, 4, 6,8,9, 10,11 12,13 ,14	P1.0_ P1.7 P3.0_ P3.7 (DIO0_DIO15)	INPUT/ OUTPUT	General Purpose digital IO pins. Weak internal pull up enabled on exit from POR or hardware reset.
20,21,22,23 24,25,26,27 33,34,35,36 37,38,39,40	18,19,20,21 22,23,24,25 30,31,32,33 34,35,36,37	16,17,181 9,22,23 24,25	17,18 ,19 20,23 ,24 25,26	P0.0_ P0.7 P2.0_ P2.7 (AIO0_AIO15)	INPUT/ OUTPUT	ADC analogue input pins. Can also be used as digital IO pins. AIO0 – AIO7 have no pull ups when using 44 or 48 pin packages.

Table 2-2 – Common Function pins

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3 Functional Description

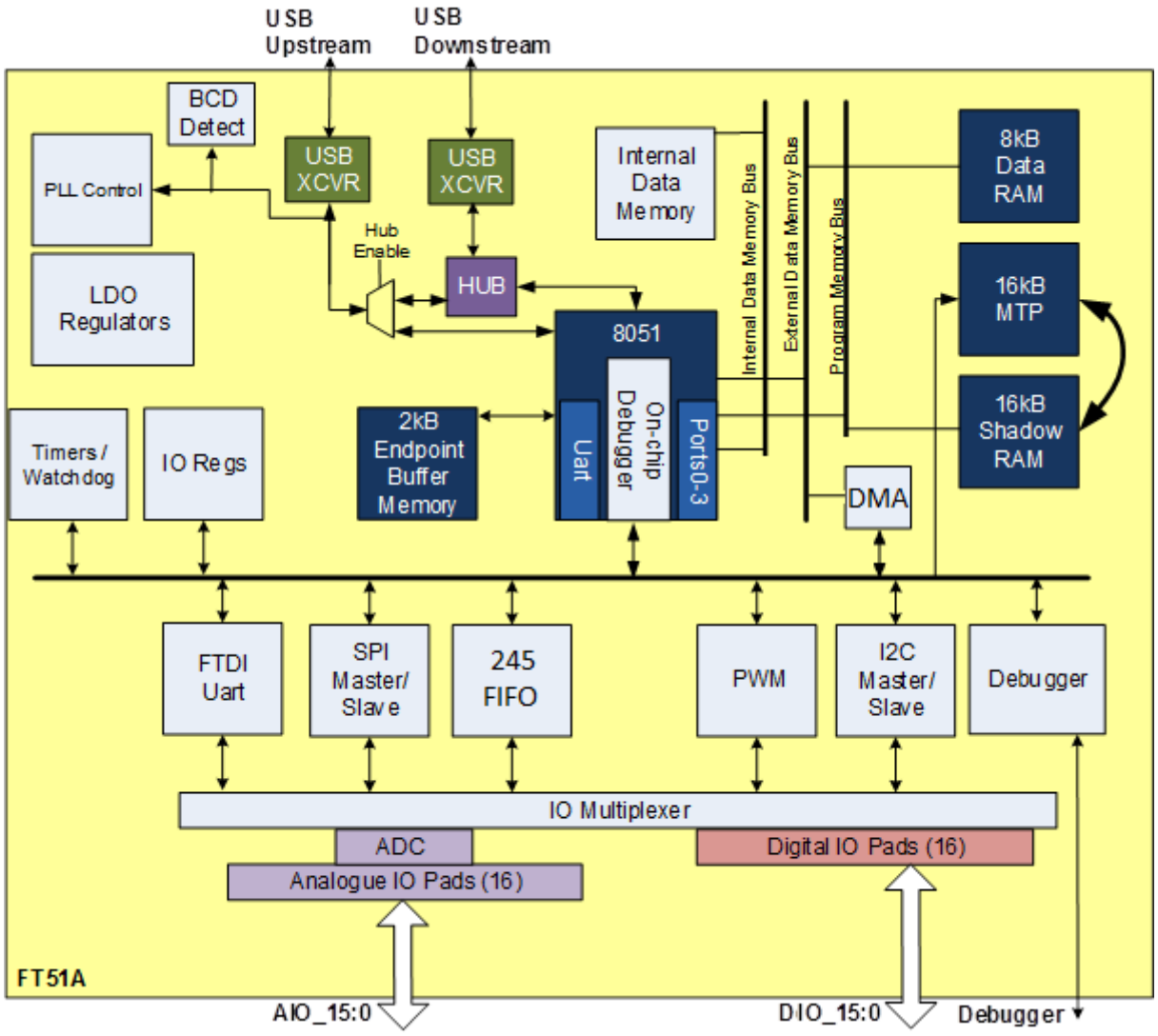

Figure 3-1 – FT51A Block Diagram

The FT51A acts as a USB hub supporting two downstream ports; the internal 8051 core and other peripherals (SPI, UART, etc.) and an external downstream port (typical devices can be a mouse, keyboard, mass storage device, etc.). The hub can optionally be disabled (under register control) resulting in the 8051 core appearing at the upstream port.

3.1 Key Features

3.1.1 Functional Integration

Fully integrated MTP memory with built in shadow RAM for fast memory access, internally generated clock, Power-On-Reset (POR) and LDO regulators.

3.1.2 8051 Core

The FT51A is based around the industry standard 8051 microcontroller capable of running at a maximum frequency of 48MHz. The core is an ultra-high performance, speed optimized single-chip 8-bit embedded controller dedicated for operation with fast on-chip memories.

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3.1.2.1 On-chip Debugger

The 8051 works with a high-performance "Hardware Assisted Debugger" which manages the communication between the core and the software.

3.1.2.2 UART / FTDI UART

There are two UARTs in the system – one designed by FTDI and the second incorporated within the 8051 core. The 8051 UART has a maximum baud rate of up to 60kbps. The FTDI UART gives speeds up to 3Mbps.

When the data and control bus are configured in UART mode, the interface implements a standard asynchronous serial UART port with full modem control. The UART can support baud rates from 183 baud to 3 Mbaud. The maximum UART speed is limited by the CPU clock. The following maximum UART speed applies:

CPU Frequency	Maximum UART Speed
48 MHz	3 Mbaud
24 MHz	3 Mbaud
12 MHz	1.5 Mbaud

3.2 Functional Block Descriptions

The following paragraphs detail each function within the FT51A. Please refer to the block diagram shown in Figure 3-1 **– FT51A Block Diagram**.

3.2.1 8051 Ports 0 - 3

The 8051 core has four 8–bit bidirectional ports: P0, P1, P2 and P3. These ports can be fully or partially mapped to external pins on the AIO and DIO bus. Firmware can change the pin mapping through IOMUX programming. Table 3-1 shows the default pin mapping for all the 4 ports on the LQFP44 and WQFN48 packages.

PIN	TYPE	DESCRIPTION
AIO7 - AIO0	Input / output	P0.7 – P0.0
AIO15 - AIO8	Input / output	P2.7 – P2.0
DIO7 - DIO0	Input / output	P1.7 – P1.0
DIO15 - DIO8	Input / output	P3.7 – P3.0

Table 3-1 – 8051 Ports

3.2.2 Timers and Watchdog

Apart from standard 8051 timers the FT51A has four general purpose 16-bit timers A, B, C and D. A 32-bit watchdog timer is also provided.

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3.2.3 PLL Control

The block provides an internally generated 48MHz clock to the system without the need of an external reference clock. This block is trimmed at factory test to 48MHz. During USB transactions the PLL will provide an accurate clock, locked to the incoming USB data rate.

3.2.4 16KB Multi-Time Programmable (MTP) memory

16K bytes of MTP memory are available for firmware programming. Code stored with the MTP memory is copied to the Shadow RAM on power up or an external reset. See section 3.2.6.

3.2.5 8KB Data RAM

8K bytes of data RAM are provided.

3.2.6 16KB Shadow RAM

To facilitate fast program memory access, limit any bottlenecks and to allow fast programming times in a debug environment, a shadow RAM exists that the CPU will run from. The Shadow RAM has the following features:

- The contents of the MTP are copied to the shadow RAM after a system reset – i.e. a POR reset or a pin reset.
- A single command (register write access) initiates a hard copy of the program memory – i.e. the contents of the shadow RAM are copied to the MTP.

3.2.7 Special Function Register

The 8051 core has a special function register area (SFR) and is limited to 128 locations. This area facilitates access to IO registers and the USB Full-Speed Device Controller command/data through in-direct addressing method.

3.2.8 IO Registers

The FT51A contains approximately 300 IO registers. See Appendix C for a full list of the IO registers.

3.2.9 LDO Regulators

The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the regulator output pin. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

The +1.8V LDO regulator generates the +1.8V supply voltage for internal digital circuits.

3.2.10 BCD Detect

Special circuitry inside the FT51A detects when the USB upstream port is connected to a dedicated charging port. When it detects that it is connected to a dedicated charging port, the FT51A can use a DIO or AIO pin to notify a microcontroller or logic on the application board which in turn controls the battery charging circuits.

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3.2.11 USB XCVR

The USB Transceiver Cell provides the USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates a 1.5kΩ pull up resistor on the USBUPDP pin.

3.2.12 IO Multiplexer

With the addition of the IO multiplexer any function can be configured to any DIO pin, excluding the analogue ADC function which is constrained to the AIO pins. All other digital functionality is recommended to map to DIO pins. The IO multiplexer allows the designer to select which peripherals are connected to which IO pins. In order to assign a signal to a particular pin, two register writes are required, one to select the signal and the other to select the IO pin. The FT51A Programmer's Guide details the pins and signals which can be connected.

The selectable peripheral interfaces are only limited by the number of IO pins available. The number of IOs available is dependent on the package type.

Table 3-2 lists the peripherals which can be multiplexed to IO and the typical number of pins required for each one. The designer can choose any mix of peripheral configurations as long as they are within the specific package IO pin count.

Peripherals	Number of pins required (typical)
UART (FTDI)	4
UART (8051)	2
ADC	1-16
8051 Port 0-3	32
SPI Master	4
SPI Slave	4
245 FIFO	12
I^2C Master	2
I^2C Slave	2
PWM	1-8

Table 3-2 – Peripheral Pin Requirements

3.2.13 I^2C Master

The FT51A provides an interface between the core and an I^2C bus. It can be programmed to operate with arbitration and clock synchronization allowing it to operate in multi-master systems. I^2C Master supports transmission speeds up to 3.4 Mb/s including Normal, Fast and High Speed modes.

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3.2.14 I²C Slave

The FT51A provides an interface between the core and an I²C bus. It can work as a slave receiver or transmitter depending on the working mode determined by the core. The core incorporates all features required by the I²C specification. The Slave supports all the transmission modes: Standard, Fast, Fast-plus and High Speed. Clock stretching is supported.

3.2.15 SPI Slave

The Serial Peripheral Interface Bus is an industry standard communications interface. Devices communicate in Master / Slave mode, with the Master initiating the data transfer.

The SPI slave module has four signals – clock, slave select, MOSI (master out – slave in) and MISO (master in – slave out).

3.2.16 SPI Master

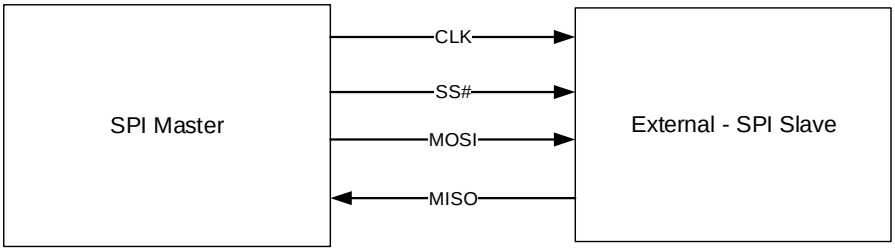

Figure 3-2 – SPI Master

The SPI Master interface is used to interface to applications such as SD Cards.

The main purpose of the SPI Master block is to transfer data between an external SPI interface and the FT51A. It does this under the control of the CPU and DMA engine via the on-chip IO bus.

The SPI master module has seven signals – clock, slave select 0..3, MOSI (master out – slave in) and MISO (master in – slave out).

The SPI Master protocol by default does not support any form of handshaking and the only available mode is unmanaged.

The SPI Master clock can operate up to half of the CPU system clock:

- CPU running at 48 Mhz would set the SPI maximum clock to 24 Mhz
- CPU running at 24 Mhz would set the SPI maximum clock to 12 Mhz
- CPU running at 12 Mhz would set the SPI maximum clock to 6 Mhz

3.2.17 Debugger

The purpose of the debugger interface is to provide the Integrated Development Environment (IDE) with the following capabilities:

- MTP Program.
- Application debug - application code can have breakpoints, be single stepped and can be halted.
- Detailed internal debug - memory read/write access.

The single wire interface has the following features:

- Half Duplex Operation
- 1Mbps speed
- 1 start bit

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- 1 stop bit
- 8 data bits
- Pull up

3.2.18 245 FIFO

The 245 FIFO interface operating in asynchronous mode has an eight bit data bus, individual read and write strobes with two hardware flow control signals.

3.2.19 PWM

The Pulse Width Modulation (PWM) block can generate a signal in which parameters such as period and duty cycle are controlled by the 8051 core. It provides 8 outputs and can generate a core interrupt if set. The main purpose is to generate PWM signals which can be used to control motors, DC/DC converters, AC/DC supplies, etc.

3.2.20 Digital IO pins

Up to 16 General Purpose digital IO pins are available depending on the package type.

3.2.21 Analogue IO pins

Up to 16 AIO pins are available depending on the package type. The pin can function in either analogue or digital mode, but not both modes at the same time.

When in analogue mode all 16 AIO pins can be configured to the ADC mode.

AIO_mode_1	AIO_mode_0	Configuration
0	0	Analogue off. If the pin is configured for digital mode, it can be controlled similar to digital IO pins.
0	1	Reserved.
1	0	ADC mode. Analogue input signal for the internal ADC convertor.
1	1	Reserved.

Table 3-3 – AIO Modes

To configure these modes, specific registers of the AIOs must be configured. On top of these modes sits a global mode which allows multiple control of AIO pins. All 16 pins can be configured depending on the package type.

3.2.22 ADC

The ADC block can convert the analogue input signal to a digital value and store the value in the registers. The ADC block can be configured to work in single-ended mode and differential mode. In single-ended mode, an input signal from any of the AIO pins can be the input to the ADC block, with the reference voltage connected to VOUT3V3. In differential mode, two AIO pins are used together to form a pair of differential inputs. The voltage difference between these two pins will be converted to digital values.

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The ADC supports single sample and global sample. In single sample mode only one selected AIO input will be sampled at a time. In global sample mode, all the selected AIO inputs will be sampled at the same time.

The sample and hold settling time of the ADC is programmable. Once conversion is done, the respective interrupt bit will be set, and an interrupt can be generated if enabled.

The accuracy of the ADC convertor is 8-bit.

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4 Device Characteristics and Ratings

4.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT51A devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
VCC5V Supply Voltage	-0.3 to +6.0	V	
VCCIO IO Voltage	-0.3 to +3.8	V	
DC Input Voltage – USB DP/DM pins	-0.5 to +3.8	V	
DC Input Voltage – digital pins (powered from VCCIO)	-0.3 to + (VCCIO +0.5)	V	
DC Output Current – Outputs	22	mA	

Table 4-1 – Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

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4.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vcc1	VCC5V Operating Supply Voltage	4.0	5	5.5	V	Normal Operation
Vcc2	VCC5V Operating Supply Voltage	3.0	3.3	3.6	V	VCC5V and VOUT3V3 pins must connect to the same 3V3 power source
Vio1	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	
Vio2	VCCIO Operating Supply Voltage	2.3	2.5	2.7	V	
Vio3	VCCIO Operating Supply Voltage	1.65	1.8	1.95	V	
Icc1	Operating Supply Current	6.5	20	28.3	mA	Normal Operation at 48MHz
Icc2	Operating Supply Current		150		µA	USB Suspend, internal clock stops
VOUT3V3	3.3v regulator output	3.0	3.3	3.6	V	VCC5V=4.0-5.5V

Table 4-2 – Operating Voltage and Current

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.9		VCCIO	V	Ioh = +/-2mA IO Drive strength = 4mA
		2.9		VCCIO	V	IO Drive strength = 8mA
		2.9		VCCIO	V	IO Drive strength = 12mA
		2.9		VCCIO	V	IO Drive strength = 16mA
Vol	Output Voltage Low			0.4	V	Iol = +/-2mA IO Drive strength = 4mA
				0.4	V	IO Drive strength = 8mA
				0.4	V	IO Drive strength = 12mA
				0.4	V	IO Drive strength*= 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.49		V	
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10		10	µA	Vin = 0

Table 4-3 – IO Characteristics VCCIO = +3V3

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25		VCCIO	V	Ioh = +/-2mA IO Drive strength* = 4mA
		2.25		VCCIO	V	IO Drive strength* = 8mA
		2.25		VCCIO	V	IO Drive strength = 12mA
		2.25		VCCIO	V	IO Drive strength = 16mA
Vol	Output Voltage Low			0.4	V	Iol = +/-2mA IO Drive strength = 4mA
				0.4	V	IO Drive strength = 8mA
				0.4	V	IO Drive strength = 12mA
				0.4	V	IO Drive strength = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	1.7			V	LVTTL
Vt	Switching Threshold		1.1		V	
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10		10	µA	Vin = 0

Table 4-4 – IO Characteristics VCCIO = +2V5

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62		VCCIO	V	Ioh = +/-2mA IO Drive strength* = 4mA
		1.62		VCCIO	V	IO Drive strength* = 8mA
		1.62		VCCIO	V	IO Drive strength* = 12mA
		1.62		VCCIO	V	IO Drive strength* = 16mA
Vol	Output Voltage Low			0.4	V	Iol = +/-2mA IO Drive strength* = 4mA
				0.4	V	IO Drive strength* = 8mA
				0.4	V	IO Drive strength* = 12mA
				0.4	V	IO Drive strength* = 16mA
Vil	Input low Switching Threshold			0.63	V	LVTTL
Vih	Input High Switching Threshold	1.17			V	LVTTL
Vt	Switching Threshold		0.77		V	
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10		10	µA	Vin = 0

Table 4-5 – IO Characteristics VCCIO = +1V8

* The IO drive strength and slow slew-rate are configurable in the IO registers.

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.8			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold			0.8	V	
Vih	Input High Switching Threshold	2.0			V	

Table 4-6 – USB DP/DM Pin Characteristics

4.3 MTP Memory Reliability Characteristics

The internal 16K Byte MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 4-7 – MTP Memory Characteristics

4.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	47.98	48.00	48.02	MHz
Duty Cycle	45	50	55	%

Table 4-8 – Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm (USB upstream port is active)

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4.5 Digital IO AC Characteristics

Please refer to the DIO section of the FT51A Programmer's Guide on how to enable / disable the Schmitt trigger, control the slew rate and determine drive strength.

Parameter	Value	load		load	
Input Timings (ns)		**0.004pF**		**1.32pF**	
		tplh	**tphl**	**tplh**	**tphl**
Schmitt Trigger	0	1.25	0.98	2.48	2.13
	1	1.27	1.08	2.51	2.24
Output Timings (ns)	**Slew Rate = Normal**	**6pF**		**120pF**	
		tplh	**tphl**	**tplh**	**tphl**
Drive Strength	00	3.33	2.37	13.34	11.13
	01	3.13	2.21	8.22	6.78
	10	3.02	2.15	6.46	5.32
	11	2.95	2.10	5.57	4.59
Output Timings (ns)	**Slew Rate = Slow**	**6pF**		**120pF**	
		tplh	**tphl**	**tplh**	**tphl**
Drive Strength	00	3.33	2.37	13.34	1.13
	01	3.33	2.37	9.24	7.81
	10	3.33	2.4	7.80	6.61
	11	3.32	2.39	7.05	5.97

Table 4-9 – Digital IO AC Characteristics

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4.6 Analogue IO Characteristics

Parameter	Description	Min	Max	Units	Conditions
INL	Non-Linearity		+/- 2	LSB	
DNL	Differential Non-Linearity		+/- 1	LSB	

Table 4-10 – ADC Characteristics

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5 USB Power Configurations

The following sections illustrate a possible USB power configuration for the FT51A. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the various package options.

5.1 USB Bus Powered Configuration

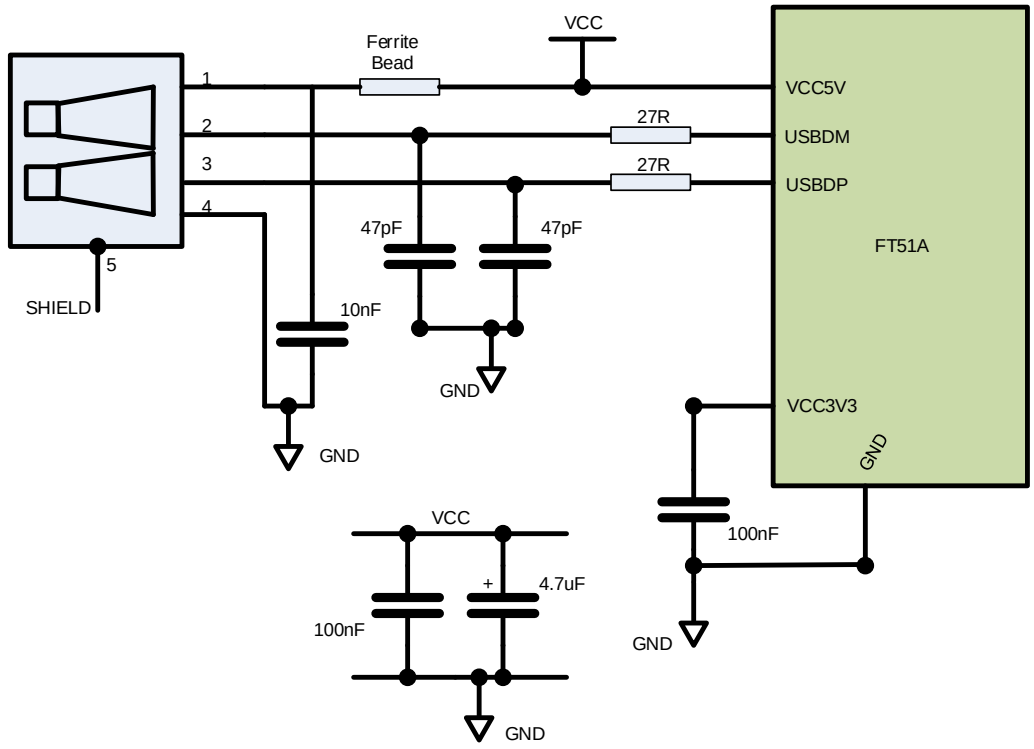

Figure 5-1 Bus Powered Configuration

Figure 5-1 illustrates the FT51A in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus powered devices are as follows –

i) On plug-in to USB, the device should draw no more current than 50mA.
ii) In USB Suspend mode the device should draw no more than 500uA.
iii) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
iv) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal MTP memory of the FT51A should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT51A and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Laird Technologies (http://www.lairdtech.com) for example Laird Technologies Part # MI0805K601R-10.

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6 Connection Examples

The following sections illustrate possible connections of the FT51A.

6.1 USB Upstream and downstream port connections (48pin package)

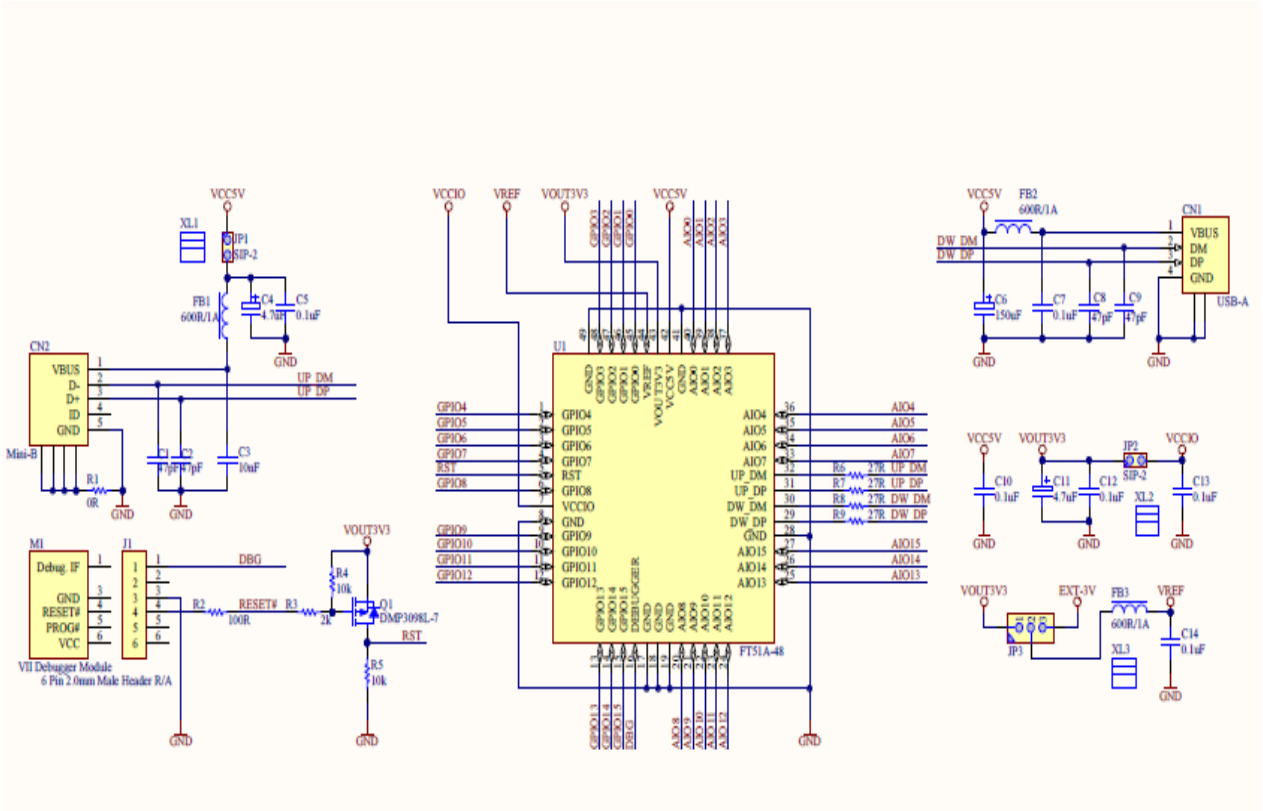

Figure 6-1 Application Example showing USB upstream and downstream connection(48pin package)

Shown above are the necessary connections to connect the upstream & downstream USB ports. The debugger module is also included for added information should it be required.

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6.2 USB Upstream and downstream port connections (44pin package)

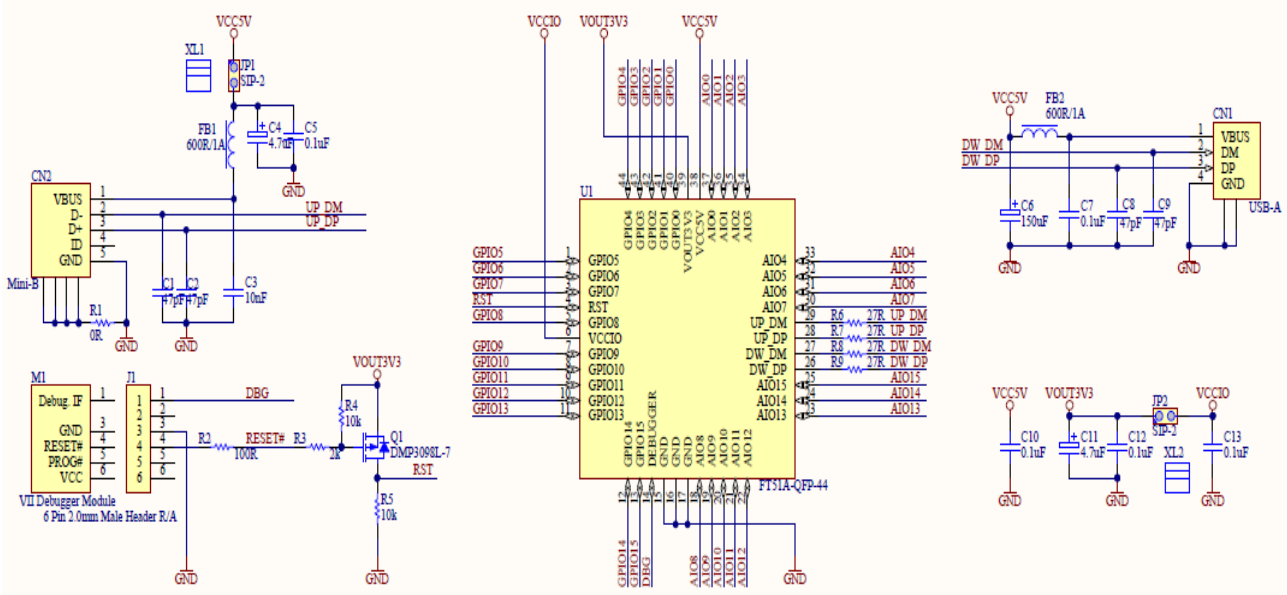

Figure 6-2 Application Example showing USB upstream and downstream connection (44pin package)

6.3 USB Upstream port connections (32pin package)

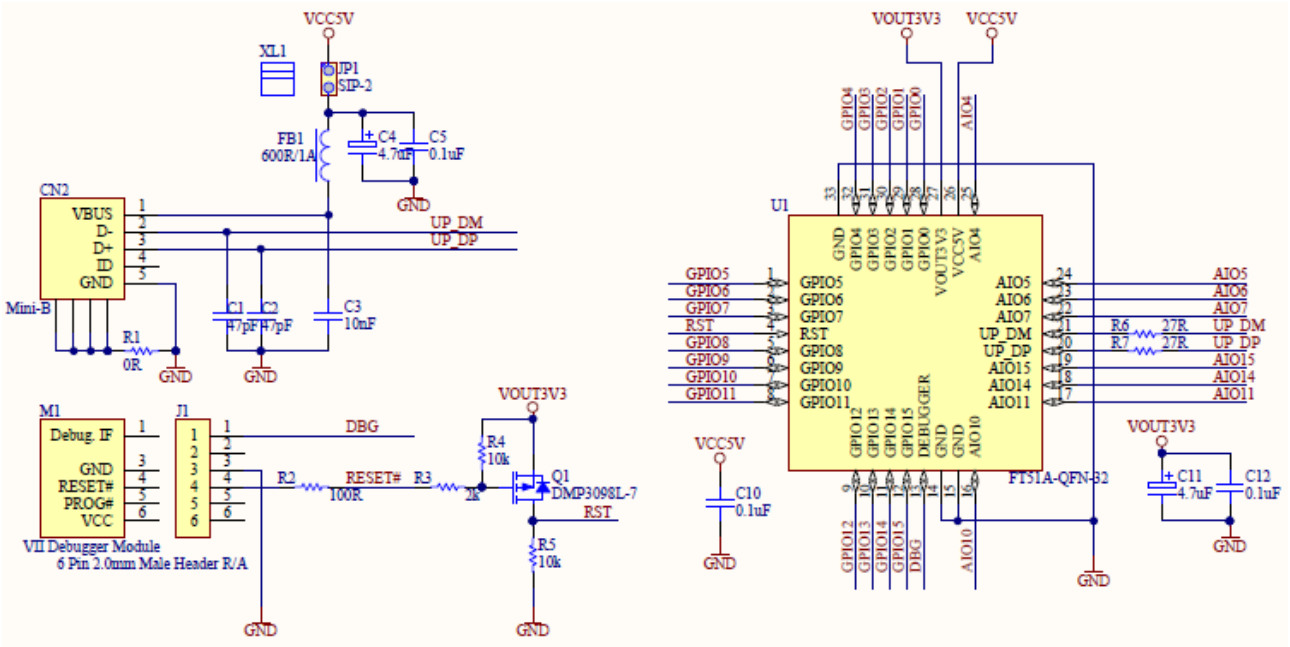

Figure 6-3 Application Example showing USB upstream connection (32pin package)

6.4 USB Upstream port connections (28pin package)

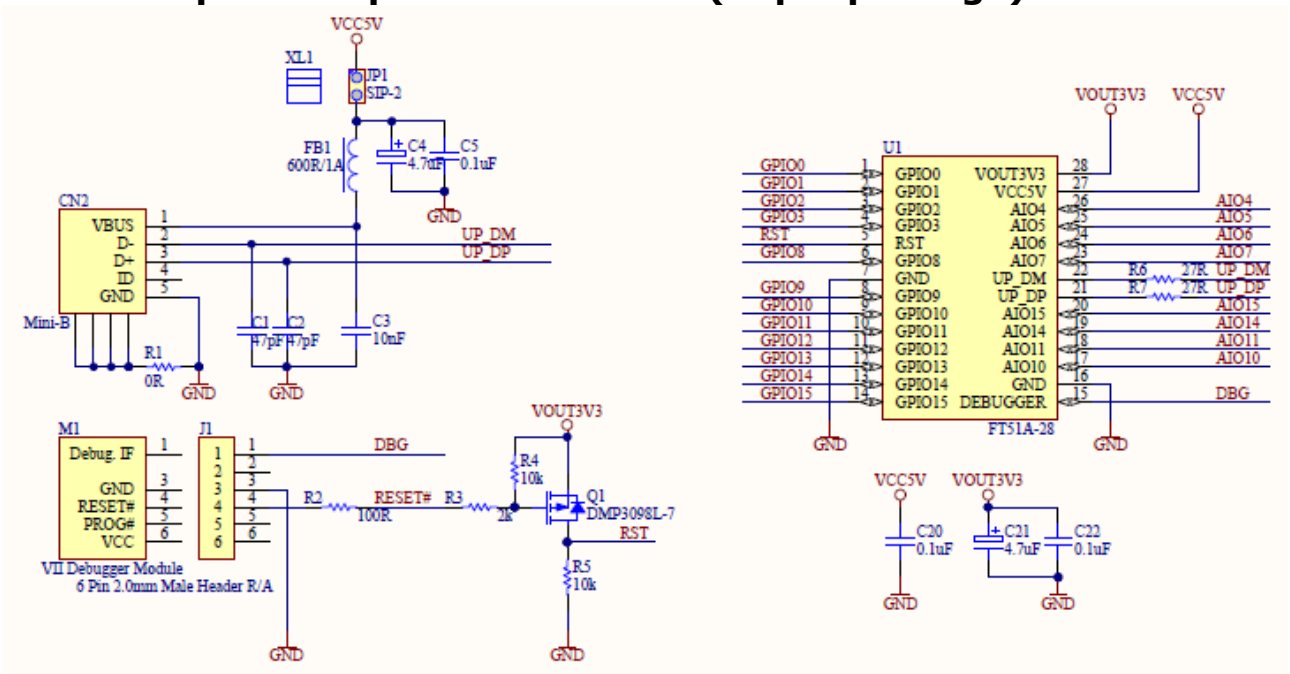

Figure 6-4 Application Example showing USB upstream connection (28pin package)

7 Package Parameters

The FT51A is available in 4 package types. The package is lead (Pb) free, RoHS compliant, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

7.1 48-Pin WQFN Package Outline

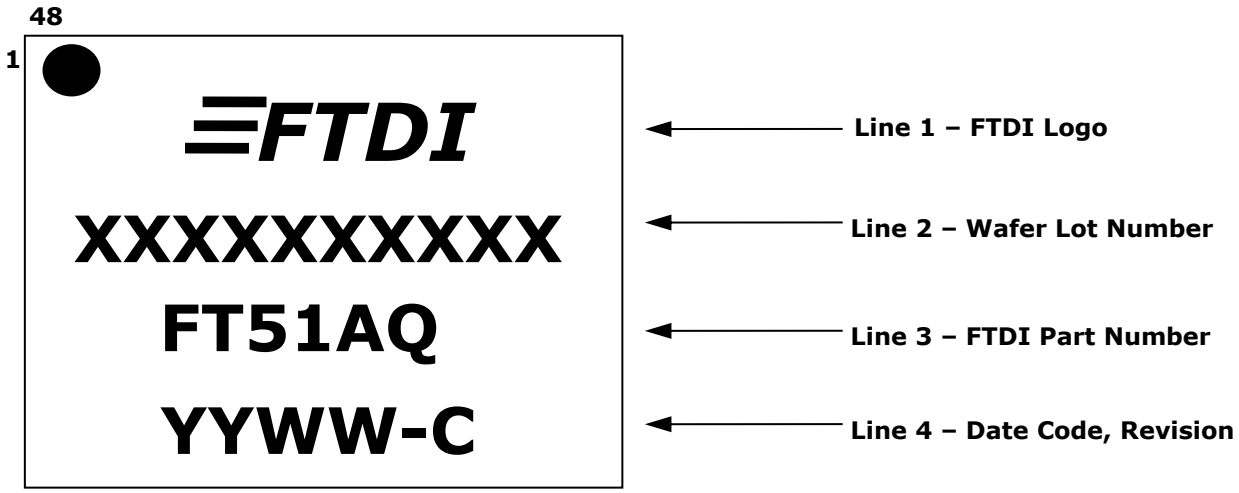

Figure 7-1 48 pin WQFN Package Marking

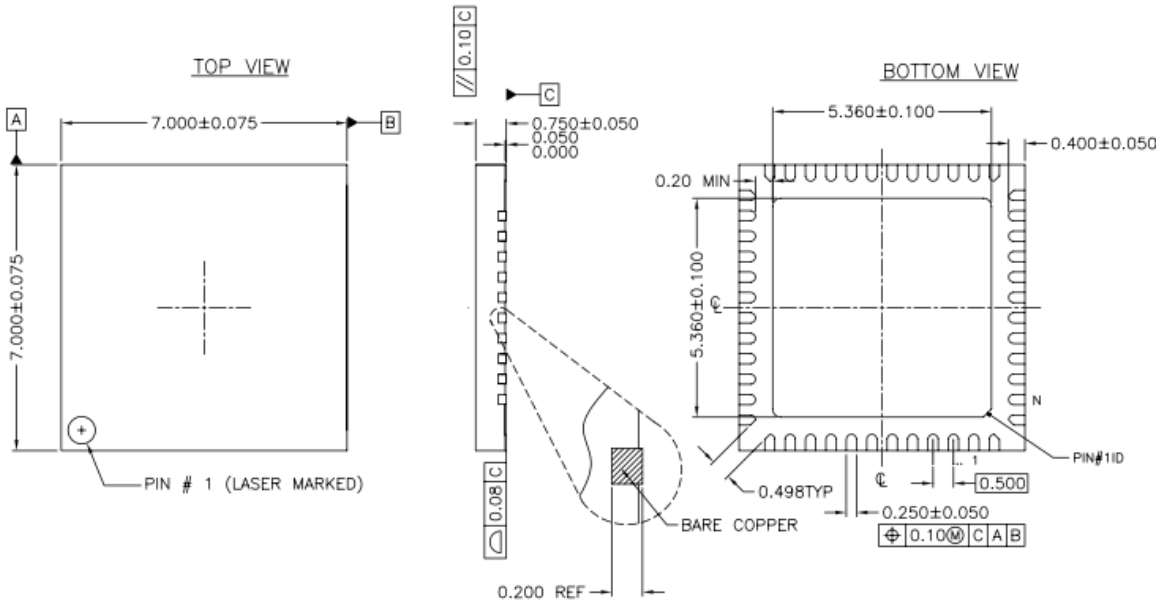

Figure 7-2 48 pin WQFN Package Dimensions

Note: The centre pad on the base of the FT51A is internally connected to ground. Dimensions are in mm.

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7.2 44-Pin LQFP Package Outline

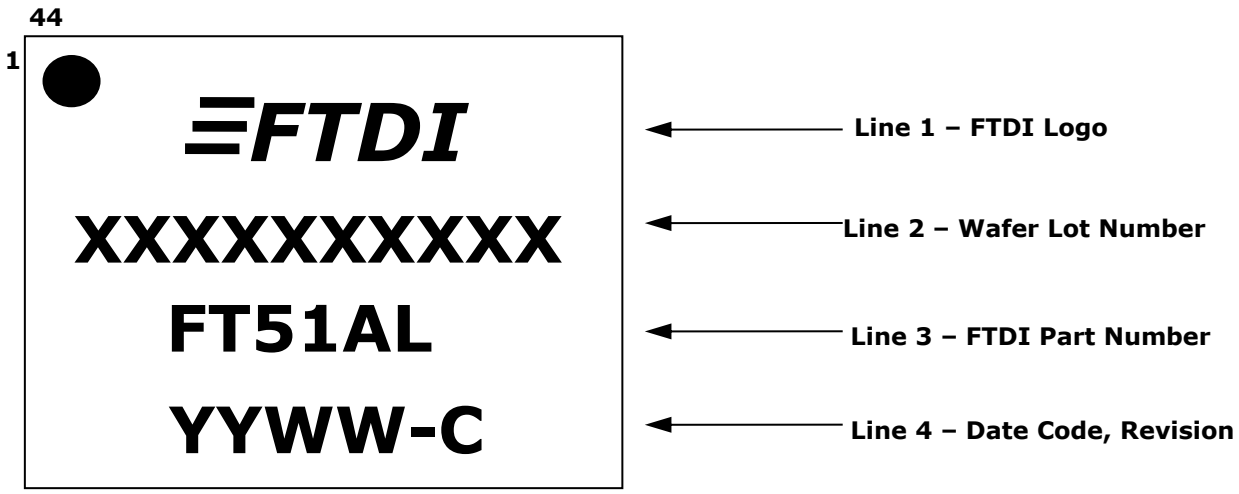
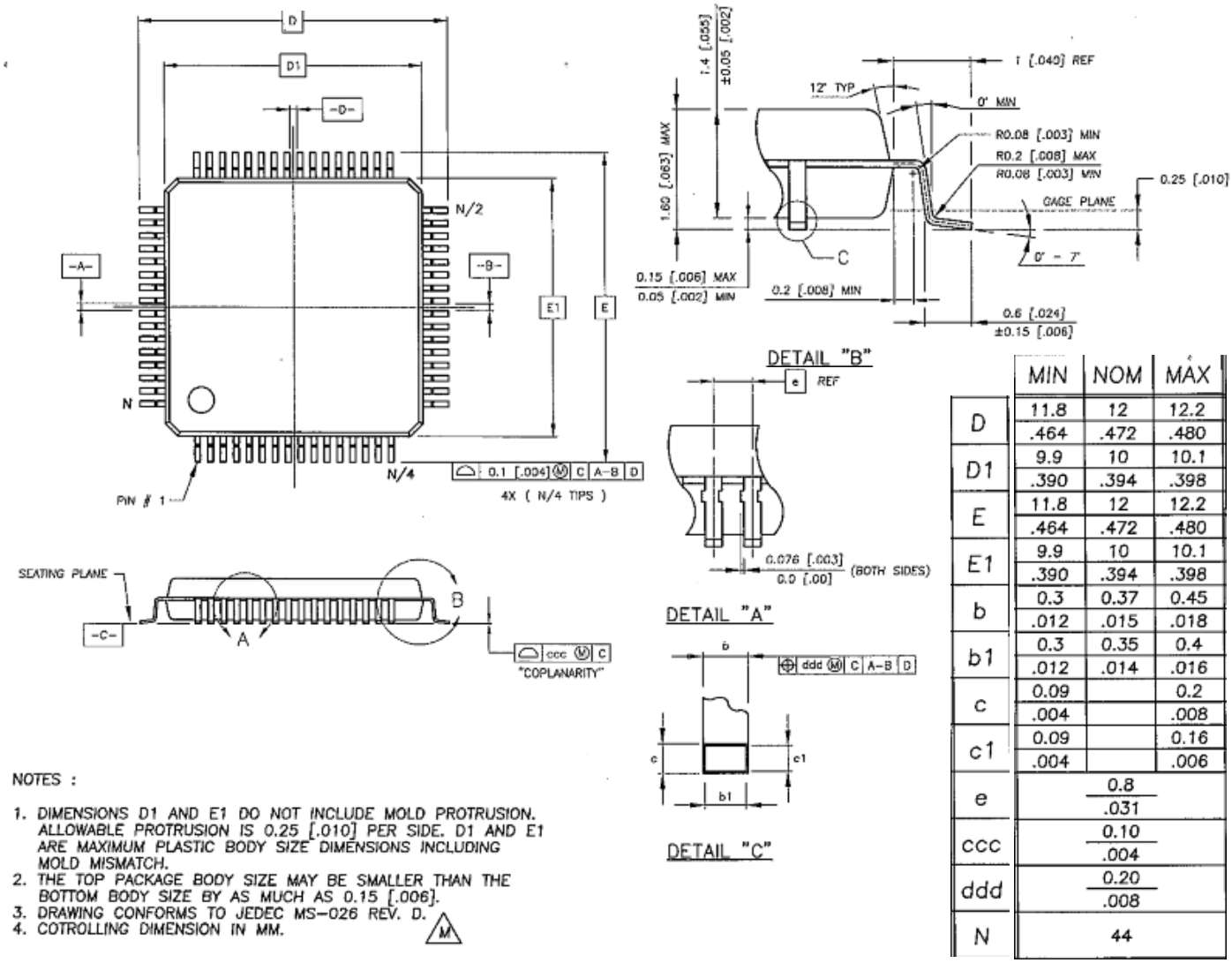


Figure 7-3 44 pin LQFP Package Marking



	MIN	NOM	MAX
D	11.8 .464	12 .472	12.2 .480
D1	9.9 .390	10 .394	10.1 .398
E	11.8 .464	12 .472	12.2 .480
E1	9.9 .390	10 .394	10.1 .398
b	0.3 .012	0.37 .015	0.45 .018
b1	0.3 .012	0.35 .014	0.4 .016
c	0.09 .004		0.2 .008
c1	0.09 .004		0.16 .006
e	0.8 .031		
ccc	0.10 .004		
ddd	0.20 .008		
N	44		

Figure 7-4 44 pin LQFP Package Dimensions

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7.3 32-Pin WQFN Package Outline

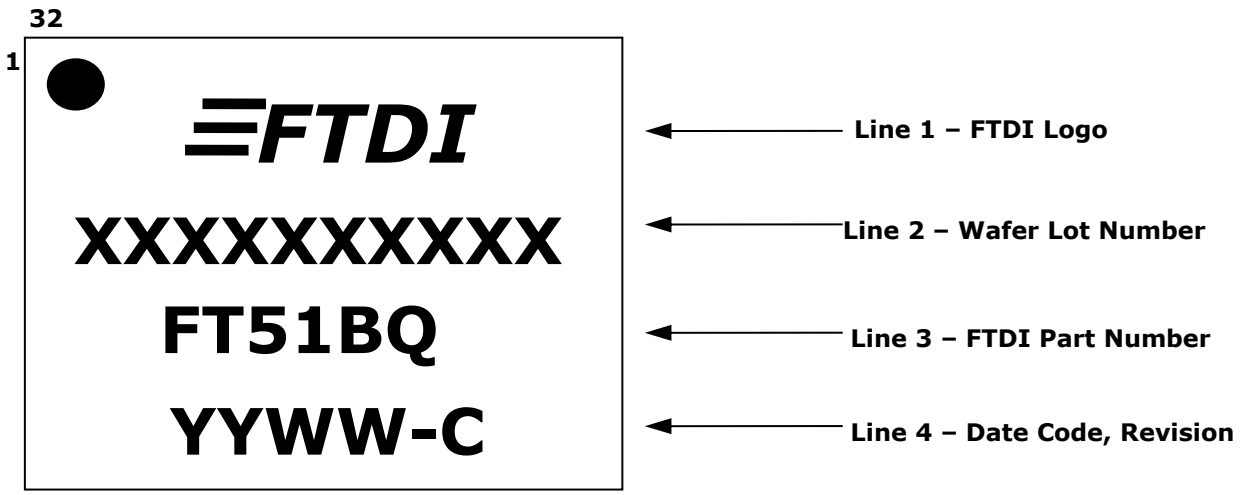
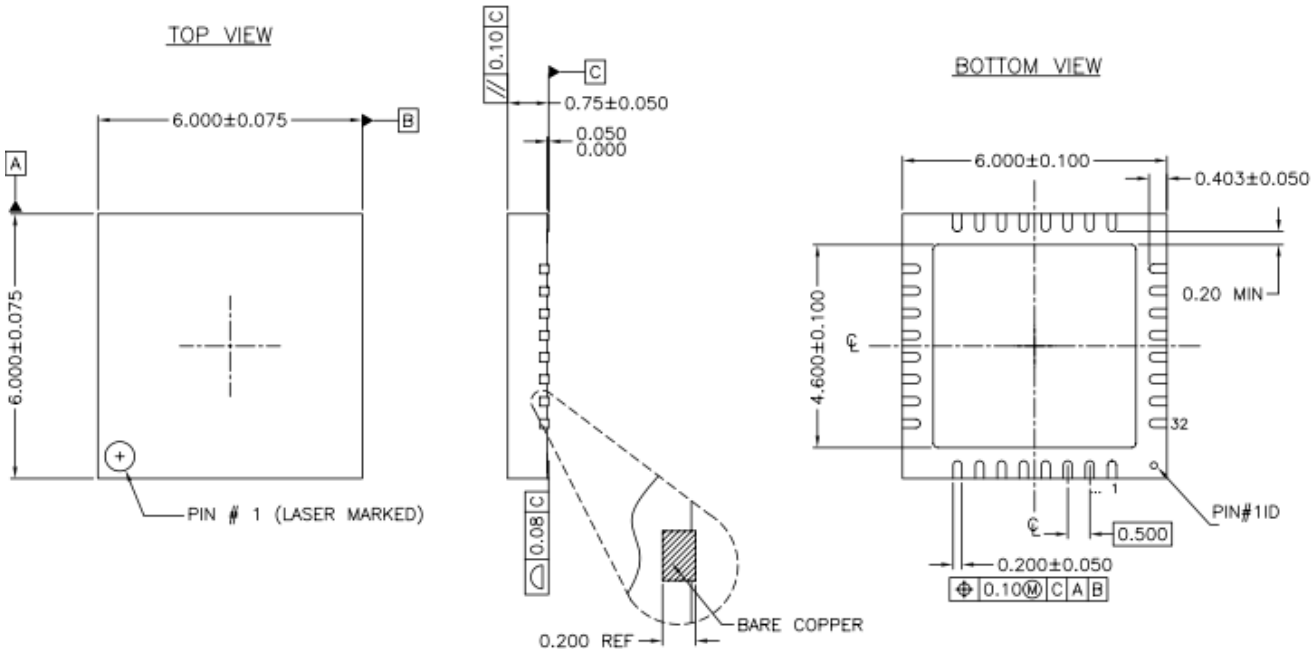


Figure 7-5 32 pin WQFN Package Marking



Note: The centre pad on the base of the FT51A is internally connected to ground. Dimensions are in mm.

Figure 7-6 32 pin WQFN Package Dimensions

7.4 28-Pin SSOP Package Outline

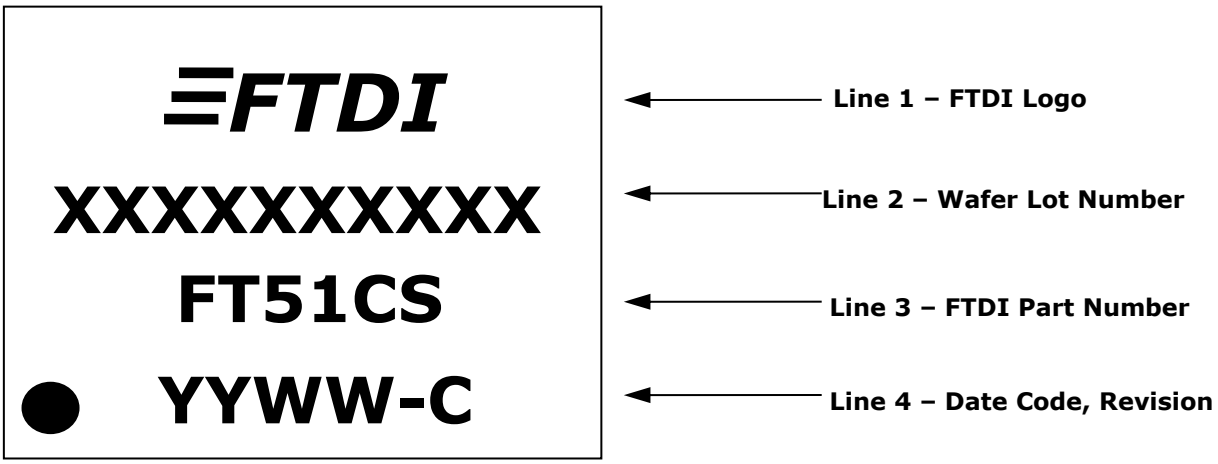


Figure 7-7 28 pin SSOP Package Marking

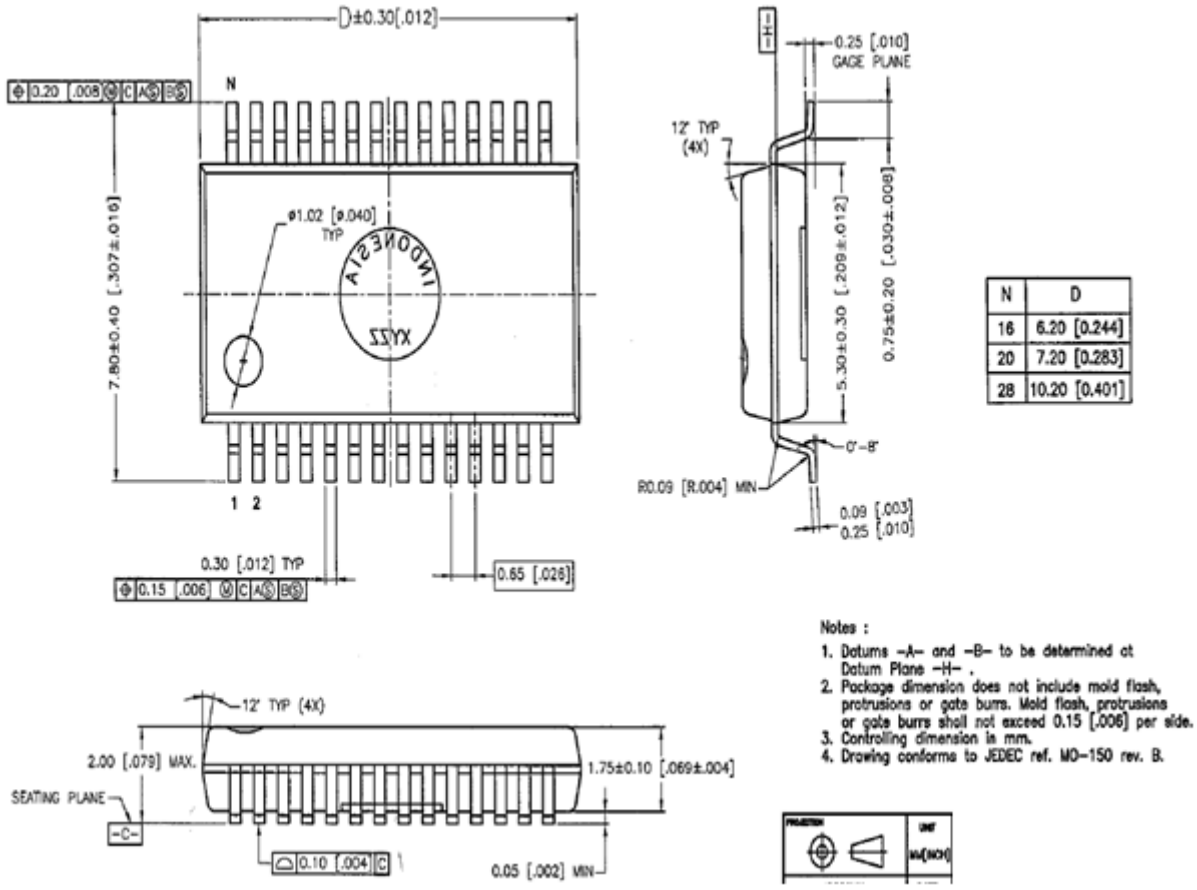


Figure 7-8 28 pin SSOP Package Dimensions

7.5 Solder Reflow Profile

The FT51A is supplied in a Pb free package. The recommended solder reflow profile is shown in Figure 7-9 FT51A Solder Reflow Profile.

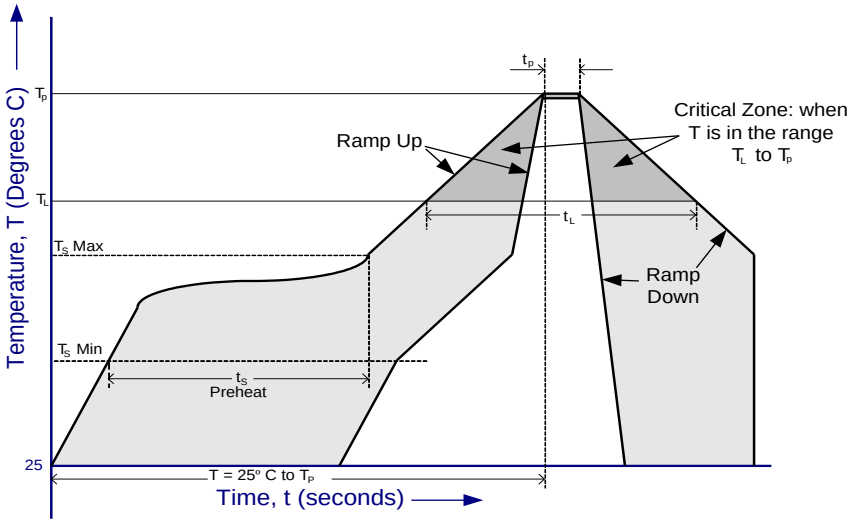


Figure 7-9 FT51A Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in **Error! Reference source not found.**. Values are shown for both a completely Pb free solder process (i.e. the FT51A is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT51A is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 7-1 – Reflow Profile Parameters

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Appendix A – References

Document References

TN_100 USB Vendor ID / Product ID Guidelines

AN_352 FT51A Installation Guide

AN_345 FT51A Keyboard Sample

AN_346 FT51A Mouse Sample

AN_347 FT51A Test and Measurement Sample

AN_348 FT51A FT800 Sensors Sample

AN_349 FT51A FT800 Spaced Invaders Sample

AN_354 FT51A Standalone Demo Application

AN_289 FT51A Programming Guide

Acronyms and Abbreviations

Terms	Description
ADC	Analog to Digital Converter
CPU	Central Processing Unit
FPGA	Field Programmable Gate Array
LQFP	Low Profile Quad Flat Package
MCU	Micro Controller Unit
PLD	Programmable Logic Device
QFN	Quad Flat No-leads
RoHS	Restriction of Hazardous Substances Directive
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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Appendix C – List of IO registers

User should refer to the FT51A Programmer's Guide for more detail.

Register Address	Register Name	Description
(0x0)	DEVICE_CONTROL_REGISTER	Device Control Register
(0x1)	SYSTEM_CLOCK_DIVIDER	System Clock Divider
(0x2)	TOP_USB_CONTROL	USB Top-level Control Register
(0x3)	PERIPHERAL_INT0	Peripheral Interrupt Status 0
(0x4)	PERIPHERAL_IEN0	Peripheral Interrupt Enable 0
(0x5)	PERIPHERAL_INT1	Peripheral Interrupt Status 1
(0x6)	PERIPHERAL_IEN1	Peripheral Interrupt Enable 1
(0x9)	PIN_CONFIG	Miscellaneous Pin Configuration
(0xA) to (0x19)	DIGITAL_CONTROL_AIO_0 to DIGITAL_CONTROL_AIO15	AIO Pins 0 to 15 Digital Control
(0x1A) to (0x29)	DIGITAL_CONTROL_DIO0 to DIGITAL_CONTROL_DIO15	DIO Pins 0 to 15 Digital Control
(0x2A)	AIO_DIFFERENTIAL_ENABLE	AIO Differential Pin Enable
(0x2B)	MTP_CONTROL	MTP Memory Control
(0x2C)	MTP_PROG_ADDR_L	MTP Program Address Lower Byte
(0x2D)	MTP_PROG_ADDR_U	MTP Program Address Upper Byte
(0x2E)	MTP_PROG_DATA	MTP Program Data
(0x34)	PIN_PACKAGE_CONFIG	Device Package Information
(0x36)	CRC_CONTROL	CRC Control of MTP Memory
(0x37)	CRC_RESULT_L	CRC Result Lower Byte
(0x38)	CRC_RESULT_U	CRC Result Upper Byte
(0x39)	SECURITY_LEVEL	Device Security Status Register
(0x40)	IOMUX_CONTROL	IOMUX Control Register
(0x41)	IOMUX_OUTPUT_PIN_SEL	Select Output Pin Number Register
(0x42)	IOMUX_OUTPUT_SIG_SEL	Select Output Signal Register
(0x43)	IOMUX_INPUT_SIG_SEL	Select Input Signal Register
(0x44)	IOMUX_INPUT_PIN_SEL	Select Input Pin Number Register
(0x48)	SPI_SLAVE_CONTROL	SPI_SLAVE Control Register
(0x4A)	SPI_SLAVE_TX_DATA	SPI Slave Transmit Data
(0x4B)	SPI_SLAVE_RX_DATA	SPI Slave Receive Data
(0x4C)	SPI_SLAVE_IEN	SPI Slave Interrupt Enable
(0x4D)	SPI_SLAVE_INT	SPI Slave Interrupt Status
(0x4E)	SPI_SLAVE_SETUP	SPI Slave Setup
(0x50)	SPI_MASTER_CONTROL	SPI_MASTER Control Register
(0x51)	SPI_MASTER_DATA_TX	SPI Master Transmit Data
(0x52)	SPI_MASTER_DATA_RX	SPI Master Receive Data
(0x53)	SPI_MASTER_IEN	SPI Master Interrupt Enable
(0x54)	SPI_MASTER_INT	SPI Master Interrupt Status
(0x55)	SPI_MASTER_SETUP	SPI Master Setup
(0x56)	SPI_MASTER_CLK_DIV	SPI Master Clock Divider
(0x57)	SPI_MASTER_DATA_DELAY	SPI Master Data Delay
(0x58)	SPI_MASTER_SS_SETUP	SPI Master Slave Select Setup
(0x59)	SPI_MASTER_TRANSFER_SIZE_L	SPI Master Transfer Size Lower Byte
(0x5A)	SPI_MASTER_TRANSFER_SIZE_U	SPI Master Transfer Size Upper Byte
(0x5B)	SPI_MASTER_TRANSFER_PENDING	SPI Master Transfer Pending
(0x60)	UART_CONTROL	UART Control Register
(0x61)	UART_DMA_CTRL	UART DMA Control
(0x62)	UART_RX_DATA	UART Receive Data
(0x63)	UART_TX_DATA	UART Transmit Data
(0x64)	UART_TX_IEN	UART Tx Interrupt Enable

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Register Address	Register Name	Description
(0x65)	UART_TX_INT	UART Tx Interrupt Status
(0x66)	UART_RX_IEN	UART Rx Interrupt Enable
(0x67)	UART_RX_INT	UART Rx Interrupt Status
(0x68)	UART_LINE_CTRL	UART Line Control
(0x69)	UART_BAUD_0	UART Baud Rate Byte 0
(0x6A)	UART_BAUD_1	UART Baud Rate Byte 1
(0x6B)	UART_BAUD_2	UART Baud Rate Byte 2
(0x6C)	UART_FLOW_CTRL	UART Flow Control
(0x6D)	UART_FLOW_STAT	UART Flow Control Status
(0x70)	TIMER_CONTROL	TIMER Top Control
(0x71) to (0x74)	TIMER_CONTROL_1 to TIMER_CONTROL_4	Timer Control Register 1 to 4
(0x75)	TIMER_INT	Timer Interrupt Status
(0x76)	TIMER_SELECT	Timer Select Register
(0x77)	TIMER_WDG	Watchdog Start Value
(0x78)	TIMER_WRITE_LS	Timer Start Value 7:0
(0x79)	TIMER_WRITE_MS	Timer Start Value 15:8
(0x7A)	TIMER_PRESC_LS	Timer Prescaler Value 7:0
(0x7B)	TIMER_PRESC_MS	Timer Prescaler Value 15:8
(0x7C)	TIMER_READ_LS	Timer Current Value 7:0
(0x7D)	TIMER_READ_MS	Timer Current Value 15:8
(0x80)	PWM_CONTROL	PWM Control Register
(0x81)	PWM_CTRL	PWM Control
(0x82)	PWM_PRESCALER	PWM PRESCALER Comparator value
(0x83)	PWM_CNT16_LSB	PWM COUNTER16 Comparator LSB value
(0x84)	PWM_CNT16_MSB	PWM COUNTER16 Comparator MSB value
(0x85) to (0x94)	PWM_CMP16_0_LSB to PWM_CMP16_7_MSB	PWM Comparator 0 LSB value to PWM Comparator 7 MSB value
(0x95) to (0x9C)	PWM_OUT_TOGGLE_EN_0 to PWM_OUT_TOGGLE_EN_7	PWM Out toggle enable register 0 to 7
(0x9D)	PWM_OUT_CLR_EN	PWM Out clear enable
(0x9E)	PWM_CTRL_BL_CMP8	PWM Control CMP8 value
(0x9F)	PWM_INIT	PWM Initialization register
(0xA0)	FIFO_CONTROL	FIFO Control Register
(0xA1)	FIFO_CTRL_STATUS	FIFO Control Status
(0xA2)	FIFO_RX_DATA	FIFO Receive Data
(0xA3)	FIFO_TX_DATA	FIFO Transmit Data
(0xA4)	FIFO_INTERRUPT_ENA	FIFO Interrupt Enable
(0xA5)	FIFO_INTERRUPT	FIFO Interrupt
(0xB0)	DMA_CONTROL_1	DMA Control Register
(0xB1)	DMA_ENABLE_1	IO DMA Enable Register
(0xB2)	DMA_IRQ_ENA_1	DMA IO Interrupt Enable & Control Register
(0xB3)	DMA_IRQ_1	DMA IO Interrupt Register
(0xB4)	DMA_SRC_MEM_ADDR_L_1	DMA IO Source Mem Addr Register (Lower Bits)
(0xB5)	DMA_SRC_MEM_ADDR_U_1	DMA IO Source Mem Addr Register (Upper Bits)
(0xB6)	DMA_DEST_MEM_ADDR_L_1	DMA IO Destination Mem Addr Register (Lower Bits)
(0xB7)	DMA_DEST_MEM_ADDR_U_1	DMA IO Destination Mem Addr Register (Upper Bits)

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Register Address	Register Name	Description
(0xB8)	DMA_IO_ADDR_L_1	DMA IO Addr Register (Lower Bits)
(0xB9)	DMA_IO_ADDR_U_1	IO DMA IO Addr Register (Upper Bits)
(0xBA)	DMA_TRANS_CNT_L_1	IO DMA Transfer Byte Count Register (Lower Bits)
(0xBB)	DMA_TRANS_CNT_U_1	IO DMA Transfer Byte Count Register (Upper Bits)
(0xBC)	DMA_CURR_CNT_L_1	IO DMA Current Byte Count Register (Lower Bits)
(0xBD)	DMA_CURR_CNT_U_1	IO DMA Current Byte Count Register (Upper Bits)
(0xBE)	DMA_FIFO_DATA_1	IO DMA FIFO DATA
(0xBF)	DMA_AFULL_TRIGGER_1	IO DMA Almost Full Flag Trigger Value
(0xC0)	DMA_CONTROL_2	DMA Control Register
(0xC1)	DMA_ENABLE_2	IO DMA Enable Register
(0xC2)	DMA_IRQ_ENA_2	DMA IO Interrupt Enable & Control Register
(0xC3)	DMA_IRQ_2	DMA IO Interrupt Register
(0xC4)	DMA_SRC_MEM_ADDR_L_2	DMA IO Source Mem Addr Register (Lower Bits)
(0xC5)	DMA_SRC_MEM_ADDR_U_2	DMA IO Source Mem Addr Register (Upper Bits)
(0xC6)	DMA_DEST_MEM_ADDR_L_2	DMA IO Destination Mem Addr Register (Lower Bits)
(0xC7)	DMA_DEST_MEM_ADDR_U_2	DMA IO Destination Mem Addr Register (Upper Bits)
(0xC8)	DMA_IO_ADDR_L_2	DMA IO Addr Register (Lower Bits)
(0xC9)	DMA_IO_ADDR_U_2	IO DMA IO Addr Register (Upper Bits)
(0xCA)	DMA_TRANS_CNT_L_2	IO DMA Transfer Byte Count Register (Lower Bits)
(0xCB)	DMA_TRANS_CNT_U_2	IO DMA Transfer Byte Count Register (Upper Bits)
(0xCC)	DMA_CURR_CNT_L_2	IO DMA Current Byte Count Register (Lower Bits)
(0xCD)	DMA_CURR_CNT_U_2	IO DMA Current Byte Count Register (Upper Bits)
(0xCE)	DMA_FIFO_DATA_2	IO DMA FIFO DATA
(0xCF)	DMA_AFULL_TRIGGER_2	IO DMA Almost Full Flag Trigger Value
(0xD0)	DMA_CONTROL_3	DMA Control Register
(0xD1)	DMA_ENABLE_3	IO DMA Enable Register
(0xD2)	DMA_IRQ_ENA_3	DMA IO Interrupt Enable & Control Register
(0xD3)	DMA_IRQ_3	DMA IO Interrupt Register
(0xD4)	DMA_SRC_MEM_ADDR_L_3	DMA IO Source Mem Addr Register (Lower Bits)
(0xD5)	DMA_SRC_MEM_ADDR_U_3	DMA IO Source Mem Addr Register (Upper Bits)
(0xD6)	DMA_DEST_MEM_ADDR_L_3	DMA IO Destination Mem Addr Register (Lower Bits)
(0xD7)	DMA_DEST_MEM_ADDR_U_3	DMA IO Destination Mem Addr Register (Upper Bits)
(0xD8)	DMA_IO_ADDR_L_3	DMA IO Addr Register (Lower Bits)
(0xD9)	DMA_IO_ADDR_U_3	IO DMA IO Addr Register (Upper Bits)
(0xDA)	DMA_TRANS_CNT_L_3	IO DMA Transfer Byte Count Register (Lower Bits)
(0xDB)	DMA_TRANS_CNT_U_3	IO DMA Transfer Byte Count Register (Upper Bits)
(0xDC)	DMA_CURR_CNT_L_3	IO DMA Current Byte Count Register (Lower Bits)

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Register Address	Register Name	Description
(0xDD)	DMA_CURR_CNT_U_3	IO DMA Current Byte Count Register (Upper Bits)
(0xDE)	DMA_FIFO_DATA_3	IO DMA FIFO DATA
(0xDF)	DMA_AFULL_TRIGGER_3	IO DMA Almost Full Flag Trigger Value
(0xE0)	DMA_CONTROL_4	DMA Control Register
(0xE1)	DMA_ENABLE_4	IO DMA Enable Register
(0xE2)	DMA_IRQ_ENA_4	DMA IO Interrupt Enable & Control Register
(0xE3)	DMA_IRQ_4	DMA IO Interrupt Register
(0xE4)	DMA_SRC_MEM_ADDR_L_4	DMA IO Source Mem Addr Register (Lower Bits)
(0xE5)	DMA_SRC_MEM_ADDR_U_4	DMA IO Source Mem Addr Register (Upper Bits)
(0xE6)	DMA_DEST_MEM_ADDR_L_4	DMA IO Destination Mem Addr Register (Lower Bits)
(0xE7)	DMA_DEST_MEM_ADDR_U_4	DMA IO Destination Mem Addr Register (Upper Bits)
(0xE8)	DMA_IO_ADDR_L_4	DMA IO Addr Register (Lower Bits)
(0xE9)	DMA_IO_ADDR_U_4	IO DMA IO Addr Register (Upper Bits)
(0xEA)	DMA_TRANS_CNT_L_4	IO DMA Transfer Byte Count Register (Lower Bits)
(0xEB)	DMA_TRANS_CNT_U_4	IO DMA Transfer Byte Count Register (Upper Bits)
(0xEC)	DMA_CURR_CNT_L_4	IO DMA Current Byte Count Register (Lower Bits)
(0xED)	DMA_CURR_CNT_U_4	IO DMA Current Byte Count Register (Upper Bits)
(0xEE)	DMA_FIFO_DATA_4	IO DMA FIFO DATA
(0xEF)	DMA_AFULL_TRIGGER_4	IO DMA Almost Full Flag Trigger Value
(0x100)	AIO_CONTROL	AIO Control Register
(0x101)	AIO_GLOBAL_CTRL	AIO Global Control Register
(0x102) to (0x105)	AIO _MODE_0 to AIO _MODE_3	Mode Select for AIO pins 0-15.
(0x108)	AIO_SAMPLE_0	Initiates a SAMPLE of AIO 0 to 7
(0x109)	AIO_SAMPLE_1	Initiates a SAMPLE of AIO 8 to 15
(0x10A)		
(0x10B)	AIO_GLOBAL_PORT_SELECT_0_7	Selects the AIOs to be included in a Global function
(0x10C)	AIO_GLOBAL_PORT_SELECT_8_15	Selects the AIOs to be included in a Global function
(0x13E) to (0x15D)	AIO_0_ADC_DATA_L to AIO_15_ADC_DATA_U	Sampled ADC data for AIO0 to AIO15
(0x16E)	AIO_INTERRUPT_0_7	Interrupt status for ports 0-7
(0x16F)	AIO_INT_ENABLE_0_7	Interrupt enable for ports 0-7
(0x170)	AIO_INTERRUPT_8_15	Interrupt status for ports 8-15
(0x171)	AIO_INT_ENABLE_8_15	Interrupt enable for ports 8-15
(0x176)	AIO_SH_COUNTER_L	Sample&Hold Settling time counter, lower 8 bits
(0x177)	AIO_SH_COUNTER_U	Sample&Hold Settling time, upper 2 bits
(0x17A)	AIO_CLOCK_DIVIDER	Clock Divider

Table 0-1 – IO Registers

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Appendix D – Revision History

Document Title	:	FT51A Advanced MCU with 8051 Compatible Core IC Datasheet
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Product Page	:	http://brtchip.com/product
Document Feedback	:	Send Feedback

Revision	Changes	Date
Version 1.0	Initial Release	2014-03-17
Version 1.1	Second Release	2014-11-05
Version 1.2	Updated Pin out Diagram	2014-12-12
Version 1.3	Updated branding from FT51 to FT51A	2015-03-23
Version 1.4	Removed DAC references	2015-11-18
Version 1.5	Updated Figure 7.8 28 pin SSOP Package Dimensions	2016-04-07
Version 1.6	Dual branding to reflect the migration of the product to the Bridgetek name – logo changed, copyright changed, contact information changed	2016-09-19

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